STUDY OF 4-BIT PIPELINE FLASH ANALOG TO DIGITAL CONVERTER USING 0.18µm CMOS TECHNOLOGY

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ABSTRACT

In this paper, effect of pipelining in 4 bit flash ADC is investigated. By adding latch staging in decoder circuit, it can improve the accuracy and meta-stability error of output signal of the flash ADC. Two stages comparator that has high speed, high level accuracy and non-compensation is used. The output of comparator is generated in form of thermometer code will be converted to binary code in decoder stage. Effect of load capacitor to the comparator stage also will be analyzed. Small value of capacitor will lead to short time transition of state, mostly because of charge and discharge of the capacitor. LTSPICE is used to design the circuit and simulate the flash ADC circuit to produce waveform of flash ADC. Based on the waveform generated, the meta-stability error of the output waveform will be analyzed. The proposed pipeline flash ADC will produce less meta-stability error than conventional flash ADC. The binary code of the conversion of input analog signal also will be analyze and tabulate.

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CHAPTER 1

INTRODUCTION

1.0 INTRODUCTION

In this chapter, the project background, problem statement, objective, scope of works and organization of project will be discussed in this chapter. Understanding about those components is very important to do this research and obtain the correct analysis.

1.1 PROJECT BACKGROUND

Commercial flash analog to digital converter appeared in instruments and modules on year 1960s and 1970s[1]. It expended very quickly during 1980s. The monolithic 8-bit flash ADC became an industry standard in digital video application. Today, the flash ADC is used in many devices such as application include digital telephones transmission, cordless phones, medical imaging, sensors, frequency modulator, demodulator and many more. All of them require high performance parameters. Consequently, different applications may require different topologies of converter[2].

Comparator circuit is very important and also the key in circuit of flash ADC architecture and strongly influences the performance of flash ADC. High degree of