IMPLEMENTING QUANTIZATION IN JPEG ENCODER USING XILINX FPGA TECHNOLOGY

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ABSTRACT

Compression of data in digital signal is a must in computer technology nowadays. Compression formats such as MPEG, JPEG, MP3 and others are widely used. Usually this compression codec are being developed using computer software and write using high level programming language such as C/C++. There are also some are being developed using RISC processor and instruction set suitable for data compression. In every format of compression data, Quantization is use as one of the main process in data compression including audio, image and video compression. The purpose of this project is to study the quantization process used in JPEG image compression and implement it on an FPGA by Xilinx. To implement quantization on an FPGA, VHDL language is used to program the behavioral logic design of quantization. Then the design is implemented on 2 Xilinx FPGA technology; Spartan and Virtex model to study the speed of processing and resource utilization on several chips on each model.

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1.0 INTRODUCTION

1.1 Background

In digital signal processing, quantization is the process of approximating a continuous range of values by a relatively-small set of discrete symbols or integer values [1]. A common use of quantization is in the conversion of a discrete signal (a sampled continuous signal) into a digital signal by quantizing. Both of these steps (sampling and quantizing) are performed in analog-to-digital converters with the quantization level specified in bits.

Quantization plays a major part in lossy data compression. In many cases, quantization can be viewed as the fundamental element that distinguishes lossy data compression from lossless data compression, and the use of quantization is nearly always motivated by the need to reduce the amount of data needed to represent a signal [3]. In some compression schemes, like MP3 or Vorbis, compression is also achieved by selectively discarding some data, an action that can be analyzed as a quantization process (e.g., a vector quantization process) or can be considered a different kind of lossy process.

In JPEG image compression, the data representing an image (typically 8-bits for each of three color components per pixel) is processed using a discrete cosine transform and is then quantized and entropy coded. By reducing the precision of the transformed values using quantization, the number of bits needed to represent the image can be reduced substantially [8].

1.2 Objectives of This Work

The objective of this work is to study, design and simulate the behavioral logic model of Quantization process uses in JPEG data compression. This project is using Very High Speed Hardware Description Language (VHDL) to design the Quantization behavioral model. The VHDL design is based on the quantization