Study of Capacitive Load effect Preamplifier Design Using SILVACO Gateway

Muhammad Taufiq Hood
Faculty of Electrical Engineering
Universiti Teknologi MARA Malaysia
Shah Alam, Malaysia
topek_hood@isiswa.uitm.edu.my

***Abstract*— This paper is to study about capacitive load effect of preamplifier design by using Silvaco Gateway. Each capacitive load can carry a specific high cut off frequency to use in any application that needed and there are any changes at frequency and transient response due to the changes of capacitive load value. The data that been taken from the two stage operational amplifier (preamplifier) with various capacitive load (10pF to 100pF) at two difference of temperature 27 and 85 °C. The result will have some suitable value of capacitive load to drive load for future use. The design of this preamplifier is using 0.18µm CMOS technology with +1.8V (V_{DD}) and -1.8V (V_{SS}) supply.**

I. INTRODUCTION

Operation Amplifier (Op Amps) was a commonly use for an analog circuits such as analog-to-digital converters. It is generally used in a negative feedback configuration which the relatively high, inaccurate forward gain can be used to achieve a very accurate transfer function [1]. Scaling down the device sizes and supply voltages makes designer use a low voltage, multistage amplifier topologies which lead to a growing of frequency compensation techniques [2]. The capacitive load is important to drive load because it often give problems such as it can reduce the output bandwidth and slew rate [3]. The stability of output needed to be optimum so that the driving load will operate smoothly. The suitable arrangement of amplifier such as multistage is widely use for low supply voltage to boost the gain by increasing the number of gain at each stage applied [4]. There are few techniques such as Nested-Miller Compensation (NMC), multi-path nested Miller Compensation (MNMC)Nested Gm-C Compensation (NGCC) [5] have been use for stabilizing multi stage amplifier [2]. There also have a continuous-time common-mode feedback where the output stage is the modified type of the simple source follower configuration [6].

In this work, proposed design is a two stage op amp using capacitor compensation also called miller compensation at differential amplifier and then it operate as operational amplifier with first order low pass filter design to run simulations.

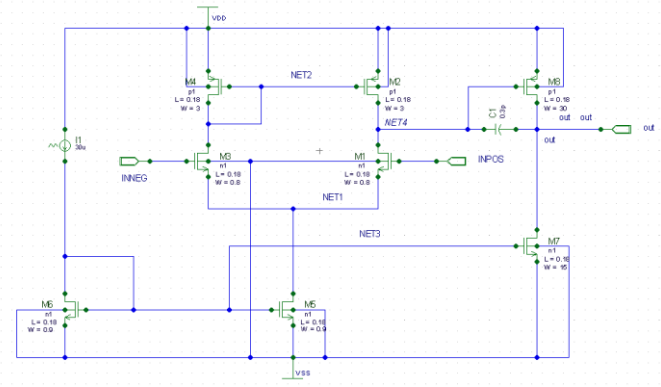

Figure 1. Preamplifier schematic design.

II. EXPERIMENTAL

The proposed preamplifier is implemented with 0.18µm CMOS technology shown figure 1, two stage amplifiers. The biasing current is set to 30µA and compensation capacitor is 0.3pF. Capacitive load value that been applied in this design are between 10pF to 100pF for observe the optimum value that can be use for the op amp.

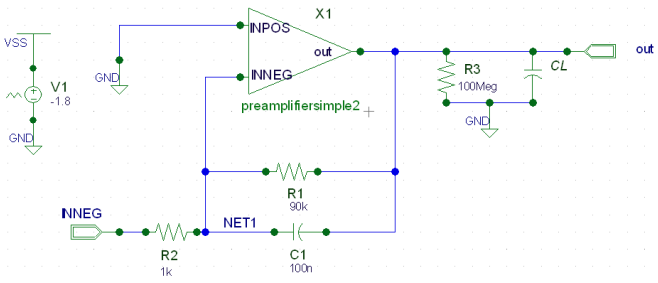

Figure 2. Op Amp schematic with low pass filter design for AC analysis.

The figure 2 shows that the proposed design to run a simulation which is inverting low pass filter op amp. To have a large gain R1 need to be larger than R2.

$$A = -\frac{R_1}{R_2} \qquad (1)$$

Where:

$$A = \frac{V_{out}}{V_{in}} \qquad (2)$$

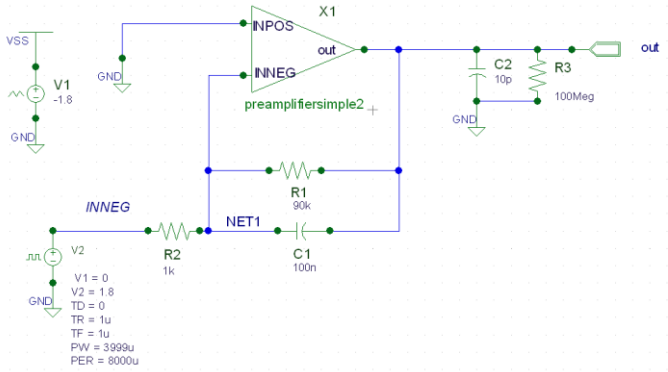

Figure 3. Op Amp schematic with low pass filter design for Transient analysis.

The input pulse width that been applied into the amplifier been set to 8000µs period, by 3999µs pulse width shown at figure 3. The output resistor needs to be bigger to balance the output to drive the load.

III. Simulation Result And Discussion

Transistor sizing shown at table 1 which there was 8 transistor been used in this design and using CMOS 0.18µm technology. The width of M8 (PMOS) is double from M7 (NMOS).

Table 1. Summary of transistor size.

Transistor	Size (w/l) µm
M1, M3	0.18/0.8
M2, M4	0.18/3
M5, M6	0.18/0.9
M7	0.18/15
M8	0.18/30

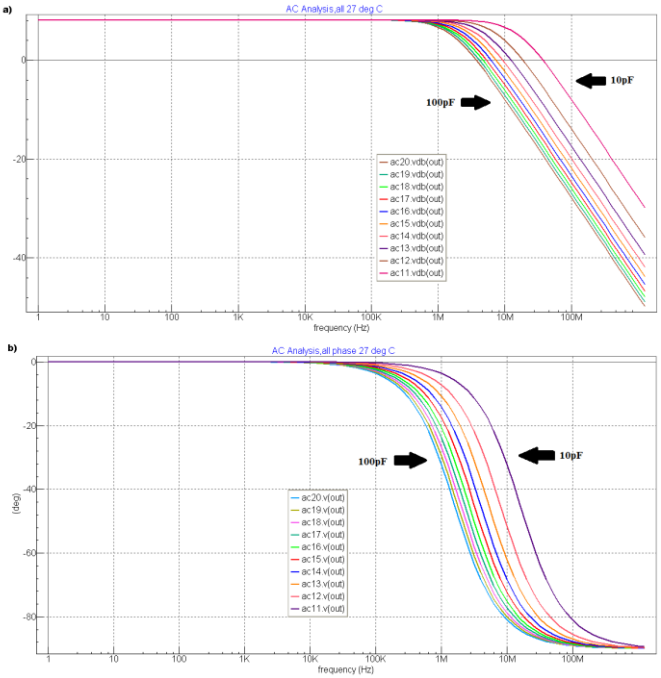

Figure 4. a) Frequency response and b) phase diagram of the amplifier for 27°C.

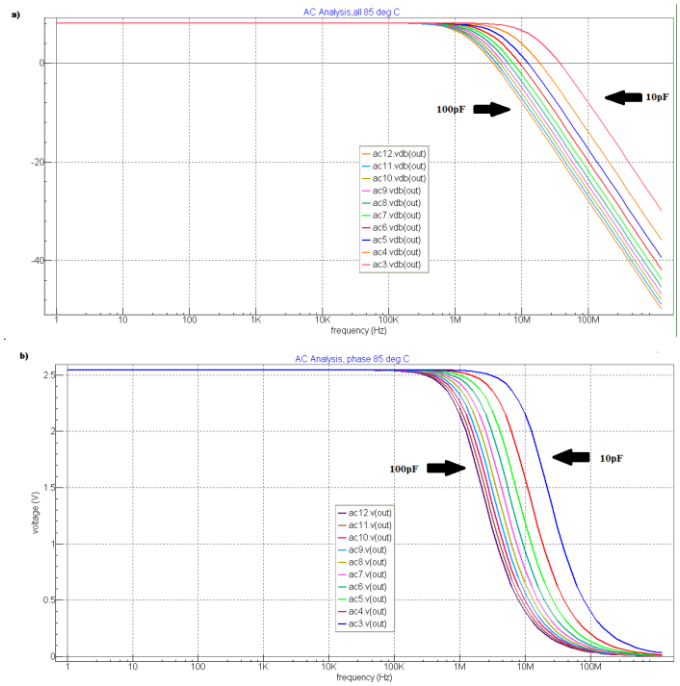

Figure 5. a) Frequency response and b) phase diagram of the amplifier for 85°C.

Result that been show from figure 4 and 5 are the merged of all capacitive value low pass result with 27 and 85°C. The big gaps of low pass frequency from 10pF to 20pF at both temperatures. These result shows that the increase of capacitive value will decrease the low pass frequency of the amplifier. The low pass frequency data for all capacitive value shown at table 2.

Table 2. Result table for low pass frequency.

C_{Load}	f_H(27°C)	f_H(85°C)
10pF	15.902MHz	15.902MHz
20pF	7.8881MHz	7.8881MHz
30pF	5.2404MHz	5.2404MHz
40pF	3.9129MHz	3.9129MHz
50pF	3.1584MHz	3.1584MHz
60pF	2.7039MHz	2.5995MHz
70pF	2.5995MHz	2.2682MHz
80pF	1.9792MHz	1.9792MHz
90pF	1.7609MHz	1.7609MHz
100pF	1.5975MHz	1.5975MHz

The stability of the signal is calculated by multiply the gain with phase. The negative result will shows that the signal at certain frequency is stable.

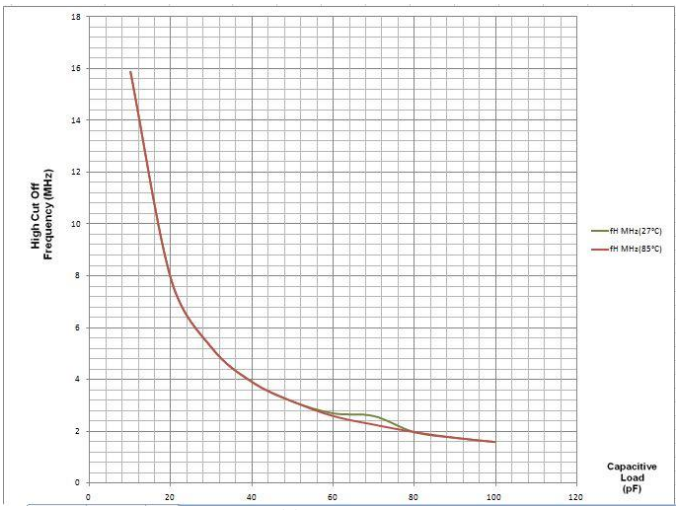

Figure 6. Graph of frequency response summary.

The graph of figure 6 shown that the curve is an inverse exponential graph with the results been taken from the table 2. The curve is effect due to the change of capacitor impedance.

$$X_C = \frac{1}{j\omega C} \qquad (3)$$

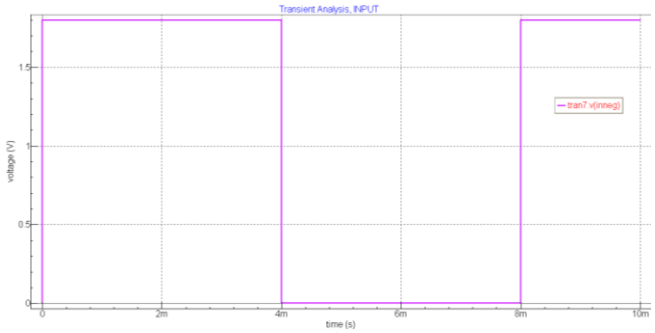

Figure 7. Input signal for transient analysis.

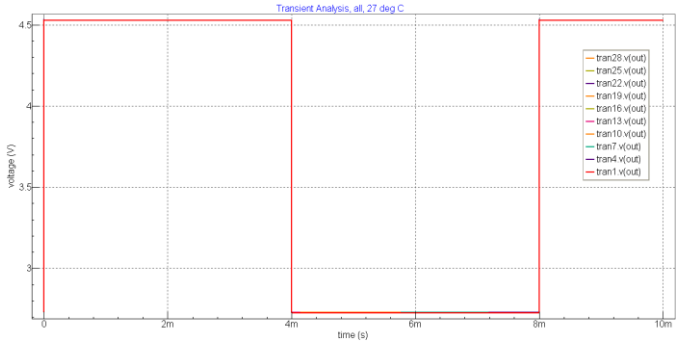

Figure 8. Output signal for all capacitive load value (27°C).

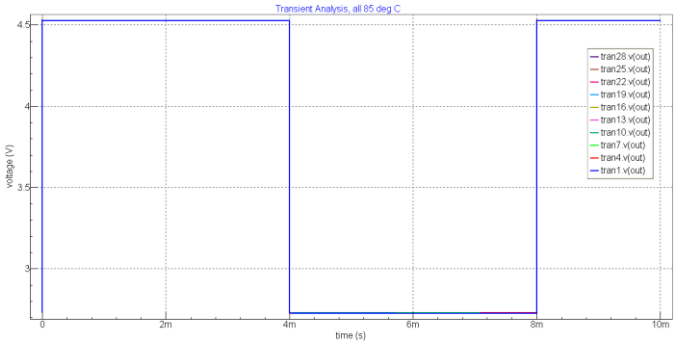

Figure 9. Output signal for all capacitive load value (85°C).

Input signal as shown at figure 7 is used to all simulation. The setting of the simulation is set with 0s time delay, output signal been produce immediately after input been applied into the op amp. Figure 8 output of temperature 27°C and figure 9 are the merged of signal at 85°C. Both signals at the same time during the change of state but at figure 10 to 13 tell a difference at the edge of rising and falling state. These figure (10 to 13) shows that there are voltage overshoot at the edge of signal at rising and fall edge. Slew rate been calculate at the overshoot voltage until the signal goes to stable condition.

$$SR = \frac{\Delta V}{\Delta t} \qquad (4)$$

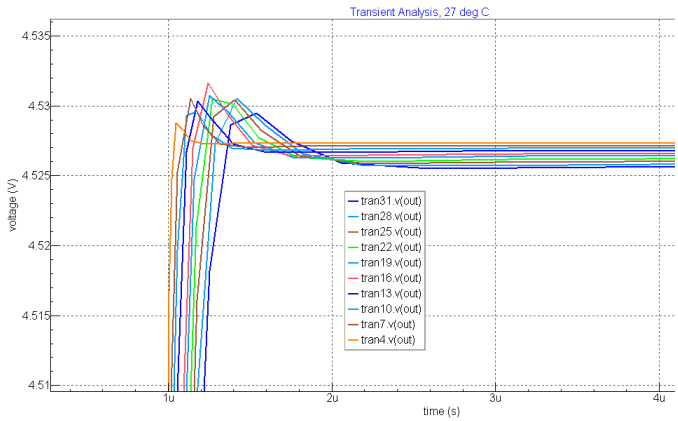

Figure 10. Output signal at rise stage (27°C).

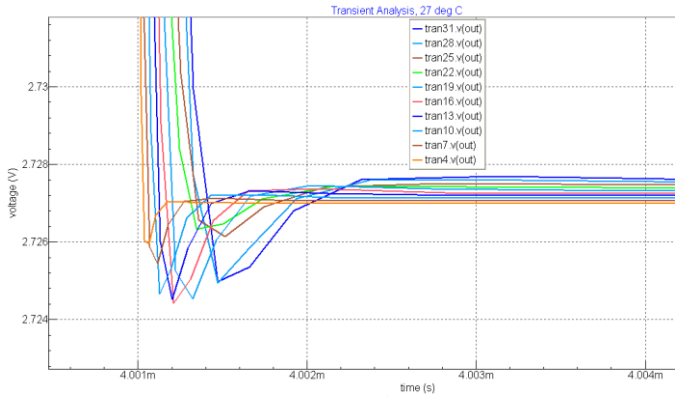

Figure 11. Output signal at fall stage (27°C).

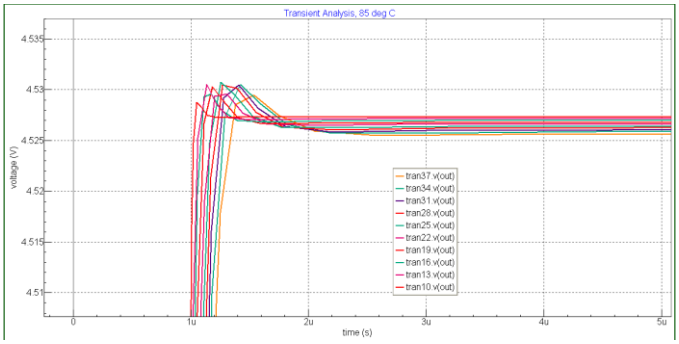

Figure 12. Output signal at rise stage (85°C).

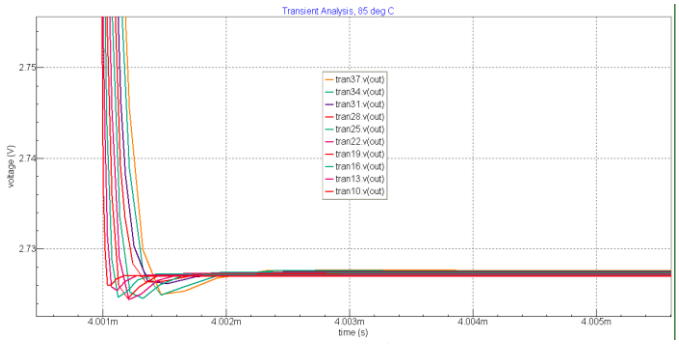

Figure 13. Output signal at fall stage (85°C).

The slew rate for 27°C is 1.705V/µs for rise stage and 1.545V/µs for fall stage. For 85°C slew rate is 1.648V/µs for rise stage and 1.5452V/µs for fall stage. Average phase margin for all result -66.765°.

The changes of capacitive load value at 85°C and 27°C outputs for frequency response are almost same this can show that the range of these temperatures doesn't affect the output result. Operational amplifier gain in dB at both analyses is 8.077dB at transient analysis result simulation and 8.111dB at frequency response simulation. The better capacitive load value for this design is at 10pF where the high cutoff frequency where it can drive load at high frequency from all value measured.

IV. Conclusion

The amplifier output change when the capacitive load value change. Each capacitive load value is use for a specific application. This study can help the future application designer to have a good selection of capacitive load value for their design. There is still needs more extensive simulation with different type of compensation of op amp and the other type of active and biasing circuit inside the op amp (CMOS differential amplifier) to differentiate the output results from the changes of capacitive load value.

References

[1] P. E. Allen and D. R.Holberg, *CMOS Analog Circuit Design*, Second Edition ed.: Oxford University Press, 2002.

[2] F. Xiaohua, *et al.*, "Single Miller capacitor compensated multistage amplifiers for large capacitive load applications," in *Circuits and Systems, 2004. ISCAS '04. Proceedings of the 2004 International Symposium on*, 2004, pp. I-493-6 Vol.1.

[3] S. Bendaoud and G. Marino, "Practical Techniques to Avoid Instability Due Capacitive Loading," 2004.

[4] L. Hoi and P. K. T. Mok, "Active-feedback frequency-compensation technique for low-power multistage amplifiers," *Solid-State Circuits, IEEE Journal of*, vol. 38, pp. 511-520, 2003.

[5] Y. Fan, *et al.*, "A multistage amplifier topology with nested Gm-C compensation for low-voltage application," in *Solid-State Circuits Conference, 1997. Digest of Technical Papers. 43rd ISSCC., 1997 IEEE International*, 1997, pp. 348-349.

[6] J. N. Babanezhad, "A low-output-impedance fully differential op amp with large output swing and continuous-time common-mode feedback," *Solid-State Circuits, IEEE Journal of*, vol. 26, pp. 1825-1833, 1991.