Simulation of 5-bit Thermometer-to-Binary Encoders for Two Different CMOS Technology

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Abstract—**Digital encoders has become bottleneck for high speed Flash-ADC architectures. This paper studies two different 5-bit thermometer-to-binary encoders that suitable for flash analog-to-digital converter. Types of thermometer-to-binary code (TC-to-BC) encoders being studied are ROM-based encoder and Multiplexer-based encoder. Both encoders are designed based on 0.18µm and 0.6µm CMOS technology each. The comparative study between 0.18µm and 0.6µm CMOS technology of both encoders design were done based on power consumption, delay analysis and layout area to determined suitable implementation for Flash ADCs. Simulation and layout design of both encoders were done on Silvaco EDA tools (Gateway and Expert).**

***Keywords*— Flash ADC, ROM, Multiplexer, TC-to-BC Encoder.**

I. INTRODUCTION

Flash analog-to-digital converter (ADC) is known for its high speed operation and simple architecture. The ADC plays an important role between analog and digital signals. It has the advantages of having very high sampling frequency and high conversion data rate, but it has the disadvantages with very large chip area, low resolution and high power consumption. Flash ADC architecture uses 2N resistors and 2N-1 comparators to convert an N-bit data. Then the outputs of comparator go to encoder to have thermometer-to-binary encoding. [1][2][3][4][7][8].

This work presents two 5-bit thermometer-to-binary encoders (TC-to-BC encoders) useful for implementation in flash ADC. Those two encoders design are ROM-based encoder and MUX-based encoder. ROM-based encoder is one of most common and straightforward design for flash ADC [1][4][8]. The main advantage of the ROM encoder approach is its regular structure that is straightforward to design, which is parallel layout architecture [1][7]. However, the conversion speed is rather slow. MUX-based encoder is another type of design for flash ADC. From research in [1][2][3], they shows trend of having MUX-based encoder producing low power consumption compared to other implementation.

In this paper, the author tried to analyse those different types of architecture of 5-bit TC-to-BC encoders suitable for the ultra-high speed flash ADCs. Two CMOS technology is implemented, which are 0.18µm and 0.6µm. The comparative study is done on average power consumption, delay time and layout area between the encoders of two CMOS technology.

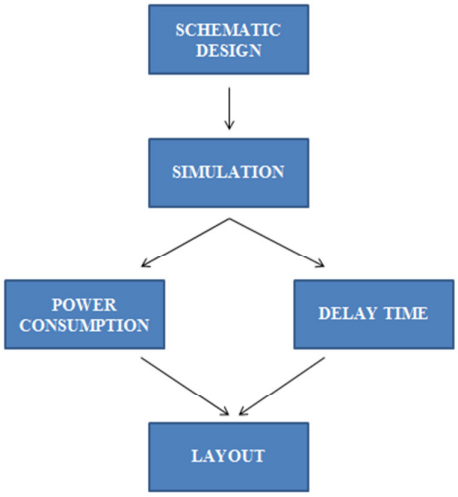

Figure 1: Flow Chart of the Project

Figure 1 shows flow chart of the project. Schematic circuit of the encoders are designed on Silvaco EDA tool (Gateway). Then, simulation of the design takes place. The simulation is done to obtained parameters for comparative study, which are power consumption and delay time. Lastly, layout of the encoders is drawn on Silvaco EDA tool (Expert) and the layout area is calculated.

This paper is divided into four main parts. In section II, the architecture of high-speed Flash ADC is reviewed. Section III considers two 5-bit TC-to-BC encoder designs, Multiplexer-based encoder and ROM-based encoder. Criterions for evaluation are explained in section IV. The results of simulation obtained are presented and discussed in section V and the conclusions in section VI.

II. FLASH ANALOG-TO-DIGITAL CONVERTER

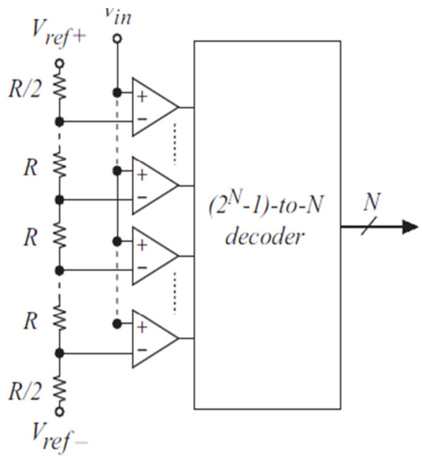

Figure 2: Illustration of a Flash ADC

Figure 2 shows a basic architecture of Flash ADC. In these circuits, the input signal is applied to the inputs of comparators, where is the number of bit. Each comparator is connected to a reference voltage commonly generated by a chain of resistors. The output of a comparator is high if the input voltage is larger than the reference voltage at the input of the comparator, otherwise the output is low. Hence the output pattern corresponds to thermometer code [1][2][3]. The output of thermometer code will go to TC-to-BC encoder. It converts the thermometer code to binary code format. Therefore the input analog voltage is represented by a binary code at the output of encoder. The relation between thermometer codes with binary codes can be seen at table 1.

TABLE 1: THERMOMETER-BINARY CODE IMPLEMENTION

Thermometer Code																															Binary Code				
R	q	Q	p	P	o	O	n	N	l	L	k	K	j	J	i	I	h	H	g	G	f	E	d	D	c	C	b	B	a	A	E	D	C	B	A
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	0	0	0	1	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	0	0	1	0	1
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	0	0	1	1	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	1	1	1
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0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	0
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	0	1	1	0	1
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1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

III. ENCODERS DESIGN FOR FLASH ADC

The thermometer coded output from the comparators is converted to binary code by a TC-to-BC encoder. These encoders can be designed in various forms, such as Multiplexer-based encoder and ROM-based encoder. In this section, two encoders design will be presented, ROM-based encoder in Sec A and Multiplexer-based encoder in Sec B.

A. ROM-based Encoder

ROM-based encoder is one of the most common and straightforward approach to encode the thermometer code [4]. The main advantage of the ROM encoder approach is its regular structure that is straightforward to design, which is parallel layout architecture. However, the conversion speed is rather slow. ROM-based encoder takes the outputs of comparator, which is the thermometer code and process it to generate binary code output.

The encoder is composed of two parts: the one-out of- N circuit (1-of-N), and the ROM encoder. At first, the thermometer code at the output of comparators is delivered to the 1-of-N. It will then detect the one-to-zero transition by using a 2-input AND gate from [8] with one input inverted. In ideal case, there will be only one logical "1" appear at the output of 1- of-N. Consequently, the output binary code is determined according to where the "1" occurred at the output of 1-of-N. Conventional NAND and INVERTER are used for one-out of- N circuit. Figure 3 and 4 show circuit of conventional NAND and INVERTER respectively.

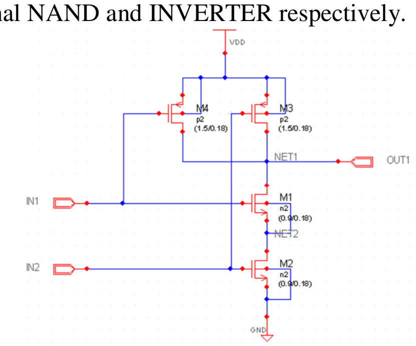

Figure 3: Conventional NAND gate

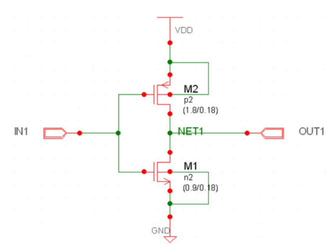

Figure 4: Conventional INVERTER gate

Pseudo-NMOS ROM approach is implemented for ROM array configuration. It is the most common style for large ROM and also offers high speed conversion [9]. In Pseudo-NMOS ROM, only one row is activated at a time. This is done by raising its voltage to Vdd, while all other rows are held at low voltage level. If an active transistor exist at the cross point of column and the selected row, the column voltage is pulled down to the low logic level. When there is no active transistor at the intersection, the voltage is pulled high by the PMOS. Width of NMOS is set to be higher than width of PMOS in order to obtain low V_{OL}. Full circuit of 5-bit ROM-based encoder is shown in figure 5.

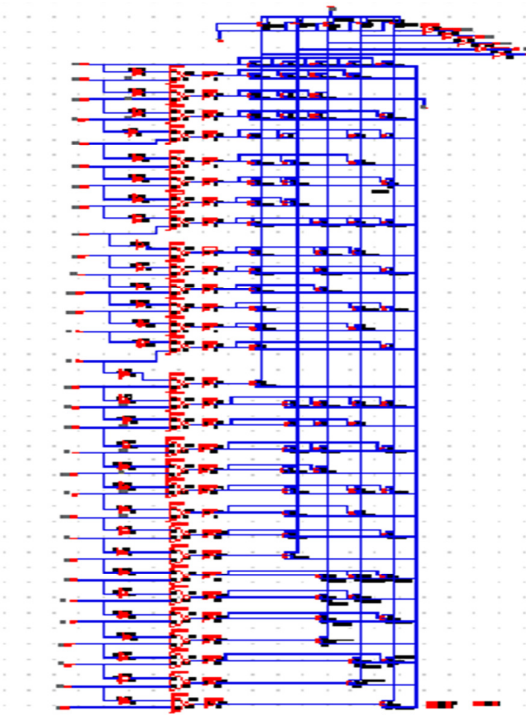

Figure 5: 5-Bit ROM-based encoder

B. Multiplexer-based Encoder (MUX)

Number of multiplexers for each stage are determined from $(2^N/2)$ +1. These stages of multiplexers are continued until there is only a multiplexer left on the last stage. For an N-bit flash ADC the most significant bit (MSB) of binary output is high if more than half of the outputs in thermometer scale are logic one [2][3]. For 5-bit MUX-based TC-to-BC encoder, MSB is same as thermometer output at $2^N/2$ bit. The second most significant bit (MSB-1) is obtained from first stage of multiplexers row. Value of MSB-1 is obtained from output of selected multiplexer in that particular multiplexer stage, which is determined by $(M+1)/2$, where M is number of multiplexers in the stage. For example, MSB-1 of 5-bit TC-to-BC encoder is determined by value of output generated by $(15+1)/2$ multiplexer, which is the 8^{th} multiplexer from the first stage. Same principle is applied in finding next most significant bit. For instance, the third most significant bit (MSB-2) is determined from the output generated from $(7+1)/2$ multiplexer, which is the 4^{th} multiplexer from second stage of multiplexers.

Due to its regular structure, it can easily be expanded to operate in a system of higher resolution than 5-bits. In this paper, the 5-bit multiplexer-based encoder is built by combination of 2:1 multiplexers and inverters. Figure 6 shows full 5-bit MUX-based TC-to-BC encoder.

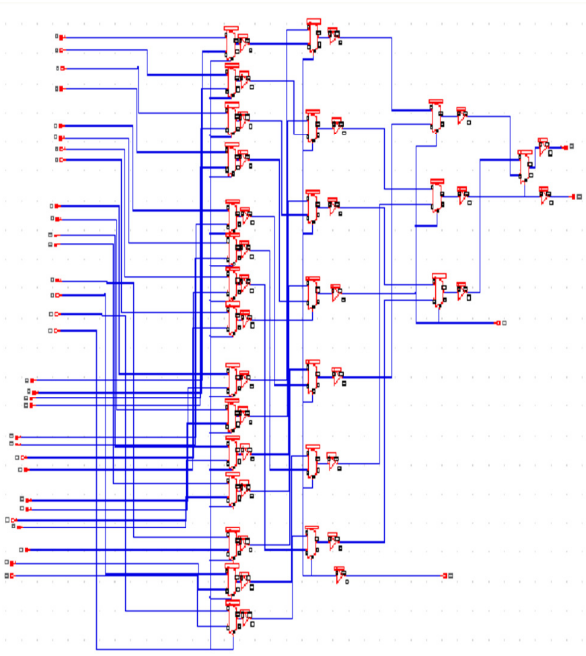

Figure 6: 5-Bit MUX-based Encoder

There is various design of 2:1 multiplexer. Research done by Ms.G.L. Madhumati et al [5] stated that Static CMOS mux offers low power consumption compared to other design. By using Static CMOS mux, it provides return to zero value which helps eliminate loss of logic level. Meanwhile, inverters design used are the same conventional inverters as discuss in part A. Figure 7 shows static CMOS 2:1 multiplexer.

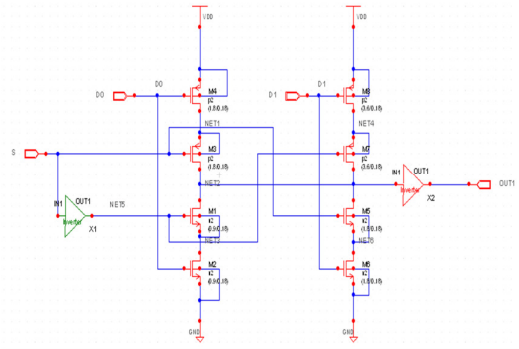

Figure 7: Static CMOS MUX

IV. CRITERION FOR EVALUATION

Parameters such as power consumption and speed define the performance of the design. Section A discuss about power consumption theory, Section B discuss on delay analysis theory while Section C on layout area theory.

A. *Power Consumption*

It is one of the important properties in VLSI design. It shows how much power will be consumes by circuit to operate. The power consumption in CMOS is quite accurately describe by [6]

$$P_g = f_d C_L V_{dd}^2 \quad (1)$$

Where $P_g$the power consumption of one gate is, f_d is the average operating frequency of that gate, C_L is the total switching capacitance of the gate, V_{dd} and is the supply voltage. For a complete chip system, containing N gates, power consumption can be estimated by

$$P_g = N f_d C_L V_{dd}^2 \quad (2)$$

B. *Delay Analysis*

Transient analysis determines how fast the design can operate. It consists of delay time between inputs injected for the decoder to generate output. Theoretically, the faster time taken to produce output, the better the design. In this paper, author focus on delay time between both encoders to produce logic high "1" when input of logic high "1" are being supplied.

C. *Layout Area*

Layout represent actual graphic of the design. Theoretically, smaller area design gives more space on wafer to fabricate more unit of that same design.

V. RESULTS AND DISCUSSION

All circuit simulation is done on Silvaco EDA tool (Gateway and Expert). Both TC-to-BC encoders are designed on 0.18µm and 0.6µm CMOS technology and simulated using 1.8V supply voltage. To establish an impartial testing environment, simulations have been carried out using a comprehensive input signal pattern which covers wide range of transition possible for the encoders. Section A discuss about power consumption, Section B discuss on delay analysis while Section C on layout area from the simulation.

A. *Power Consumption*

Series of analysis is done to obtain power consumption. Then, average power consumption is calculated and tabulated. Table 2 shows comparative study of power consumption between present works with previous works from Ms.G.L. Madhumati et al [1]. Figure 8 gives clearer view of average power consumption simulation.

TABLE 2: COMPARISON OF AVERAGE POWER CONSUMPTION OF BOTH ENCODERS.

No.	Encoder Type	Power Consumption	
		Previous Work (0.18µm)	Present Work (0.6µm)
1	ROM-based encoder	2.3341 e-004	7.88894 e-005
2	MUX-based encoder	2.5408 e-005	2.45855 e-005

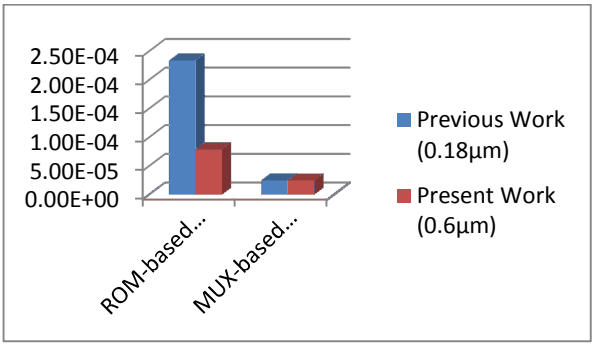

Figure 8: Average Power Consumption Vs Type of Encoder

From analysis done, it clearly show that MUX-based encoder dominates in term of average power consumption compared to ROM-based encoder for both 0.18µm and 0.6µm CMOS Technology.

For ROM-based encoder, 0.6µm design gives less average power consumption compared to 0.18µm design by 66.2%. As for MUX-based encoder, 0.6µm design also produces less average power consumption compared to 0.18µm design by 3.24%

In term of 0.6µm CMOS technology design, MUX-based encoder generated less average power consumption compared to ROM-based encoder by 68.84%. This result follows trend from previous work [1][2][3] that show pattern of having MUX-based encoder as low power consumption design.

B. *Delay Time*

Series of transient analysis is done to gain speed of the encoders in term of delay time. For comparative purpose, both encoders design are being given same input pattern to produce same equal output waveform. Table 3 shows

comparison of delay time for both encoders on two different CMOS technology. Figure 9 gives clear view on delay time analysis.

TABLE 3: COMPARISON OF DELAY TIME OF BOTH ENCODERS.

No.	Encoder Type	Delay Time	
		0.18µm	0.6µm
1	ROM-based encoder	0.0907n	1.0705n
2	MUX-based encoder	0.3140n	3.7140n

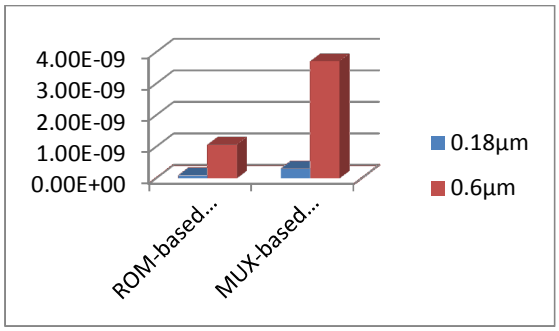

Figure 9: Delay Time Vs Type of Encoder

Simulation shows that ROM-based encoder design gives faster delay time compared to MUX-based encoder for each 0.18µm and 0.6µm design.

For ROM-based encoder, 0.18µm design reduces delay time compared to 0.6µm design by 91.53%. While for MUX-based encoder, 0.18µm design gives faster delay time compared to 0.6µm by 91.55%.

In term of 0.18µm CMOS technology category, ROM-based encoder generates faster delay time compared to MUX-based encoder by 71.12%. Whereas in term of 0.6µm CMOS technology design, ROM-based encoder also produces lower delay time compared to MUX-based encoder by 71.18%. 0.18µm CMOS technology offers around 71.15% average delay time reduction.

Figure 10 shows transient simulation done by injecting input from input 1 up to input 9, while figure 11 shows transient analysis by injecting input from input 1 to input 22. Output that generated from both encoders follow table 1 of thermometer-binary code implementation

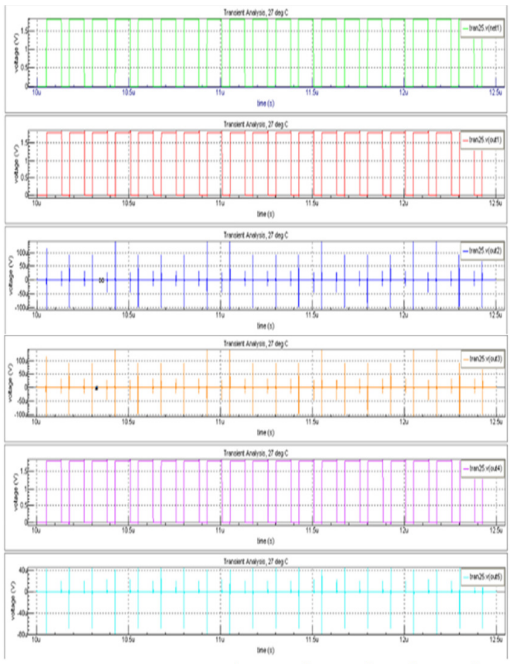

Figure 10: Transient Simulation of ROM-based Encoder

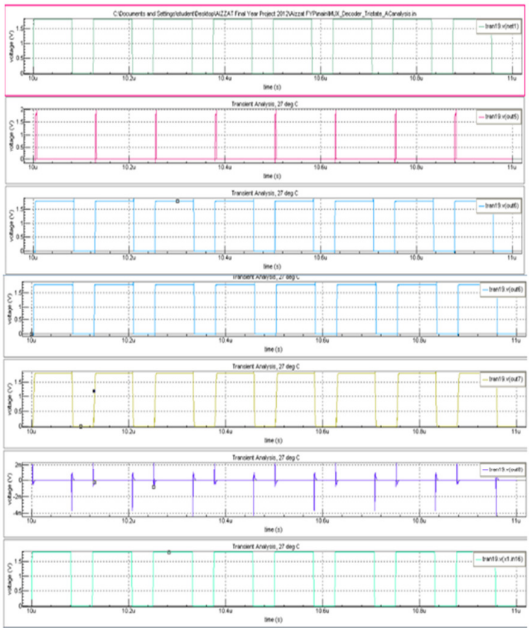

Figure 11: Transient Simulation of MUX-based Encoder

C. *Layout Area*

Layouts of both encoders are performed on Silvaco EDA tool (Expert). Both encoders are designed based on 0.6µm CMOS Technology. Comparative analysis is done on layout area of both encoders. Table 4 shows comparison of layout are for both 0.6µm ROM-based encoder and MUX-based

encoder. Figure 12 presents graphical view on the layout area comparison.

TABLE 4: COMPARISON OF LAYOUT AREA OF BOTH ENCODERS.

No.	Encoder Type	Layout Area (0.6µm)
1	ROM-based encoder	5375.97µm^2
2	MUX-based encoder	7402.91µm^2

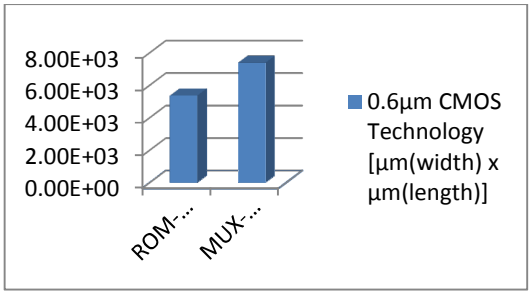

Figure 12: Layout Area for 0.6µm design

From the layout designed, ROM-based encoder produces less layout area compared to MUX-based encoder by 27.38%. Figures 13 and 14 show layout designs of ROM-based encoder and MUX-based encoder respectively based on 0.6µm CMOS technology. Designed ROM-based encoder has parallel layout follows pattern from [7]. Whereas worked MUX-based encoder shows pattern of having regular structure as claimed in [2].

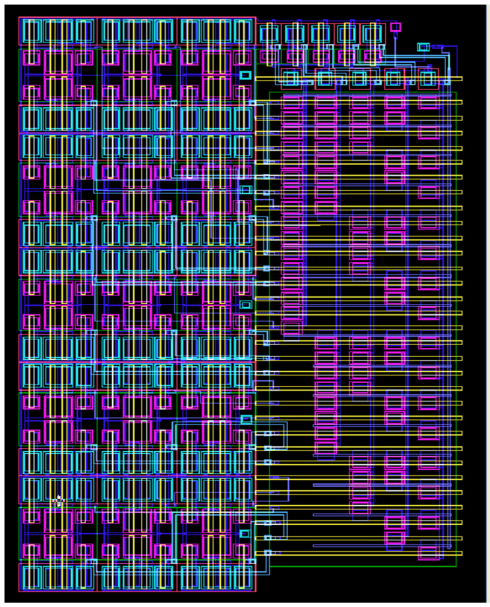

Figure 13: ROM-based Encoder Layout

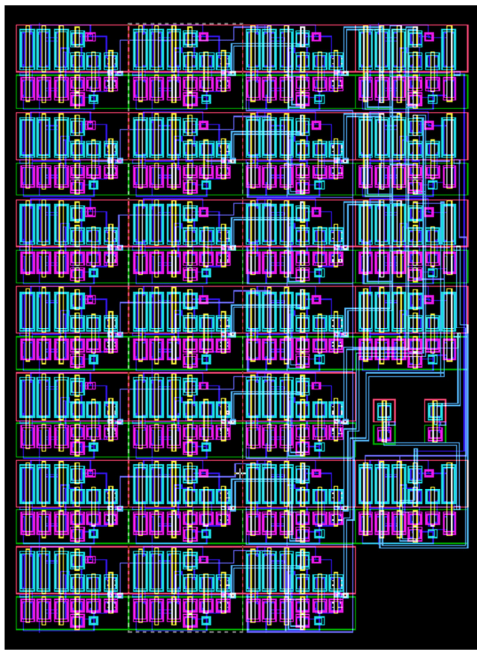

Figure 14: MUX-based Encoder Layout

VI. CONCLUSION

According to the simulation results, MUX-based encoder offers low average power consumption compared to MUX-based encoder for both CMOS technology. 0.6µm design shows to have better low power consumption compare to 0.18µm design. In term of speed, ROM-based design is better than MUX-based encoder for both CMOS technology. Layout size of ROM-based encoder is smaller than MUX-based encoder.

It can be concluded that in term of CMOS technology, 0.6µm offers low power consumption but has issue with speed, whereas 0.18µm CMOS technology gives better speed but not efficient in power consumption. Meanwhile for TC-to-BC encoder design itself, MUX-based encoder is more efficient in term of low power consumption whereas ROM-based encoder is better when higher speed and smaller area are concern for Flash ADC.

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