Simulation of Double Stack Dielectric MOS Capacitor

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Abstract - **This paper report the study about the relationship of Capacitance-Voltage (C-V) characteristics in MOS structure devices characterization. All these things are completely related with the experimental of double stack dielectric MOS capacitor in range of 35nm, 65nm and 95nm Silicon Oxide thickness neither calculated or simulated capacitance. This project has been done by absolutely using TCAD Silvaco software. Athena and Atlas tools modules are most important simulators used that had been calibrated and manipulated in this experiment in order to fabricate the better MOS capacitor with the fabricated industry standard sample from wafer Fabrication Lab. For this study, three operating modes under negative and positive bias such as the accumulation, depletion and inversion also have been put to prove the capacitance value obtained. Besides that, few parameters that have been considered and pay more attention which are the dielectric permittivity, thickness of dielectric, and MOS structure's area in this experiment to relate both of the calculated value and simulation output of the total capacitance from fabricated sample.**

Keywords —**Capacitance-Voltage Characteristics (C-V Curve); Metal–Oxide–Semiconductor (MOS) Capacitor; dielectric thickness, dielectric permittivity; area**

I. INTRODUCTION

Actually to understand the concept of ideal MOS capacitor structure is rather similar with the MOSFET or its specific name is Metal Oxide Semiconductor Field-Effect Transistor, but the structure of MOS capacitor absolutely having no source and drain region in their structure.

Furthermore, the MOS capacitor also a combination between the oxide capacitance and depletion layer capacitance which is connected in series. It also one of the basic electronics components in era of advanced technology nowadays which are consist of a MOS basic structure as shown in the Figure 1 below.

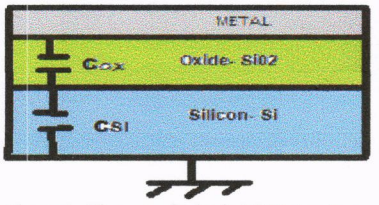

Figure 1 :Diagram of a basic MOS structure

In order to produce this basic MOS capacitor structure, the surface of the silicon is well oxidized to develop an insulating layer of Silicon Oxide (SiO2).

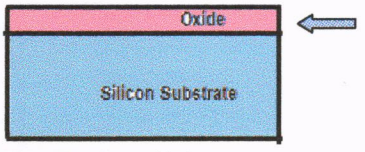

Figure 2 : After oxidation process

Then, the top of the MOS structure will be formed as a metal contact, and usually it using metal from Aluminium (Al), this layer also known as a gate. Besides that, to the backside of that semiconductor structure also was developed an Ohmic contact on the second metal layer that also known as the bulk, body or source. As well known, the major section of MOS technology is the metal–oxide–semiconductor structure layer respectively which is the most used in the semiconductor field device structure today. Owing to this case, when the structure completely connected as two terminal device, by means of the one electrode was connected to the metal layer and then the other one will connected to the bulk of semiconductor, and it will results as a voltage dependent capacitance [1] . As well as the integrated circuit (IC) devices today actually are reduced to get better performance, by give emphasize the consumption of electric power used is waning, then gate oxide thickness is also diminish specifically depends on the needs [2][3]

But for this study, the experimental work was focused on and how to find the suggested value of the capacitance for the physical parameters of three different inputs thickness of Silicon dioxide (SiO2), in order to achieve the target of the measured capacitance of fabricated sample from the real wafer fabrication lab from the industry. As well as the integrated circuit (IC) devices today actually scaled down to get better performance, the gate dielectric thickness also decreased specifically depends on the needs by emphasize the lower power consumption used [2][3]. For that purposed, the gate oxide thickness decreased with the flow of technology according to chart stated in The National Technology Roadmap for the Semiconductor [4].

As the oxide layer thickness has been reduced, their performance that results from the capacitance also has been drastically increased. By replacing the silicon dioxide material with Silicon Nitride Si_3N_4 with the constant thickness 65nm which having larger dielectric constant will drive the gate capacitance increased without the same leakages affect that across the part of dielectric area. The material of Si_3N_4 film also absolutely suitable acts as a capacitor storage [5].

The MOS behavior described above is well-illustrated by C-V measurements, which are made by applying to the structure high or low frequency sinusoidal voltages of several mili-volts superposed to the bias voltage. For C-V analysis, from the previous literature reports the significant study of the relationships between capacitance and voltage. The simulated C-V characteristics are totally useful to face with experimental data for different types of MOS structures with the various types of semiconductors and dielectric stacks [6].

II. THEORETICAL BACKGROUND

The MOS capacitor structure of the capacitance is depends on the voltage (bias) on the gate. That capacitance represent as a voltage applied function to the capacitor, which is the most important consideration in MOS structure. This is because the capacitances that have different bias modes provided an important characterization, which are quite useful to check the capacitor structure's condition and quality.

For a MOS structure, there are three modes of operation regions that are considered, which is accumulation, depletion and inversion bias modes. These operations of three modes as well as the charge distributions are related with each other as Figure 2 shown below.

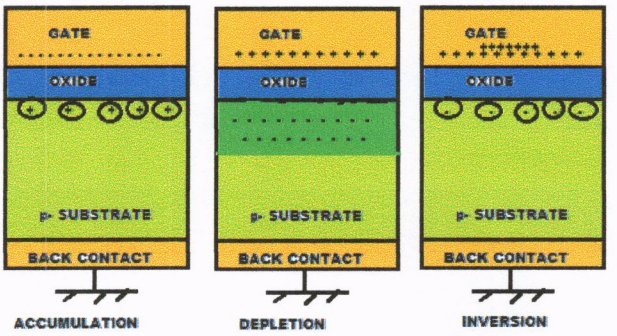

Figure 3: Movement of charges in NMOS Capacitor (with subtstrate of *p*-type) for accumulation, depletion and inversion condition modes.

In accumulation region is for ($V_G < V_{FB}$) condition. Flat Band voltage also known as V_{FB} is the "built-in" voltage of the MOS structure. We already know that the capacitance is huge because the holes will attracts by negative charge on the surface of gate layer and will created a +ve mobile carriers charge to interface from p-substrate to the oxide of semiconductor. At this condition, that MOS is characterized a structure that look like parallel plate capacitor that piling the holes up at the surface. Therefore the low frequency capacitance, C_{LF} and high frequency capacitance, C_{HF} equals to equation (1) [7].

$$C_{LF}=C_{HF}=C_{ox} \qquad (1)$$

Where:
$$C_{OX}=\frac{\varepsilon_o \varepsilon_{ox} A}{t_{ox}}, \text{ [F/m]} \qquad (2)$$

Depletion occurs for ($V_{FB} < V_G < V_T$), when the voltage that becomes positive and then the channel will depleted the holes or in other word when operation start increasing the voltage across the capacitor. The mobile of holes push by the positive charge into the bulk substrate. Then, the mobile carriers are depleted at a negative charge and interface region, due to the ionized acceptor ions, will leave in space charge region. Then, the signals also slowly varied then will allow the time to generate the minority carriers, so that drift current will across the depletion region, and it will recombine. The voltages will divide the accumulation and depletion region and it referred as Flat band voltage, V_{FB} [8].

In this study, for high frequency of 1MHz, the capacitance value obtained with maximum depletion width range. It also will occur at voltage exceed the value of threshold voltage, Vth [9].

For inversion modes, while the interface on the oxide layer of the semiconductor, there will emerged a negative charged that drive to the depletion layer. Then, this inversion layer is about when the positive gate voltage (Vg>0), that have been interfaced with the minority carriers [8].

II. METHODOLOGY

In this study, to developed whole process in order to obtained the MOS capacitor structure or simulation itself required to use both of TCAD modules : ATHENA simulator for simulation process module besides the ATLAS simulator is for module of device simulations.

For the process simulation part, in order to design this MOS capacitor structure in 2-dimensional (2D) is fully used the ATHENA framework simulator. For simulation part, it totally focused on how to obtained the suggested value for the physical parameter of three different input. It also need to fulfill the specification target between the measured capacitance and the fabricated sample from industry wafer fabrication.

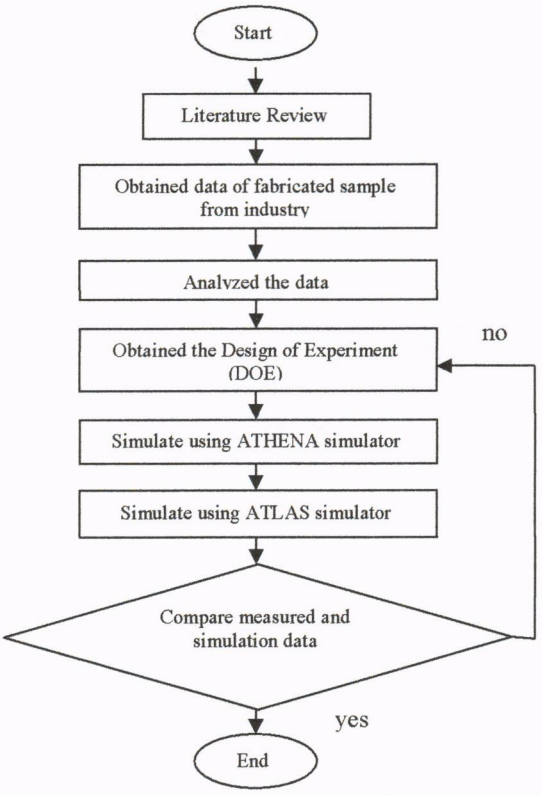

Figure: Flowchart of process flow

III. SIMULATION AND DISCUSSION

A. Gate Oxide Thickness by Diffuse Time manipulations

Diffuse Time, (min)	Gate Oxide Thickness (nm)
1.0	11.52
4.0	24.96
6.0	32.48
8.0	39.48
10.0	46.17
13.0	55.80
15.0	61.01
17.0	65.84
20.0	72.81
22.0	77.31
26.0	85.99
30.0	94.27
31.0	96.24

Table 1: Changing the diffuse time affected on the Gate Oxide Thickness

Based on Figure 3 above, by using Silvaco ATLAS shown that the manipulated diffuse time in minute, results in different oxide thickness have been obtained. In addition, the temperature and pressure value left constantly. Owing to that, the temperature and gas pressure value is 1092.05 C and 1.14953 atm respectively, with the percentage of HCL is 3.55764.

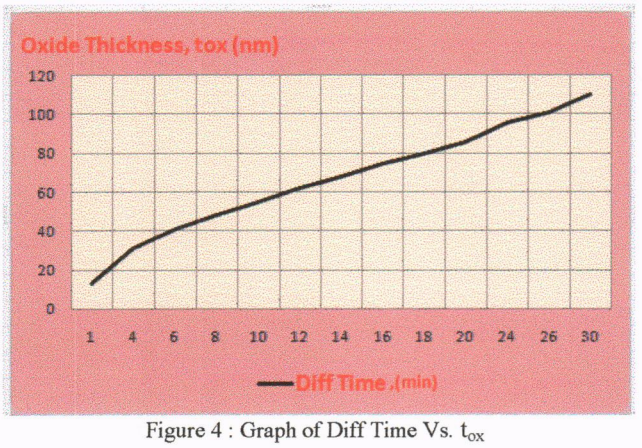

Figure 4 : Graph of Diff Time Vs. t_{ox}

B. Device Simulator

Silvaco TCAD tools software were used to fabricate the process of device simulation by using both simulator which are ATHENA and ATLAS module. For this project, there are some operation that mixed up to developed this double stack dielectric MOS capacitor structure.

The process of device simulation which are involved is for purposed in define the meshes process, perform deposition process, to developed the gate oxidation layer, p-well annealing process, nitride deposition process, nitride deposition annealing process, aluminum deposition process , and plotting the tonyplot structure process [9]. By using ATHENA simulator, the structure of double stack dielectric of MOS capacitor was obtained as shown in Fig 5.

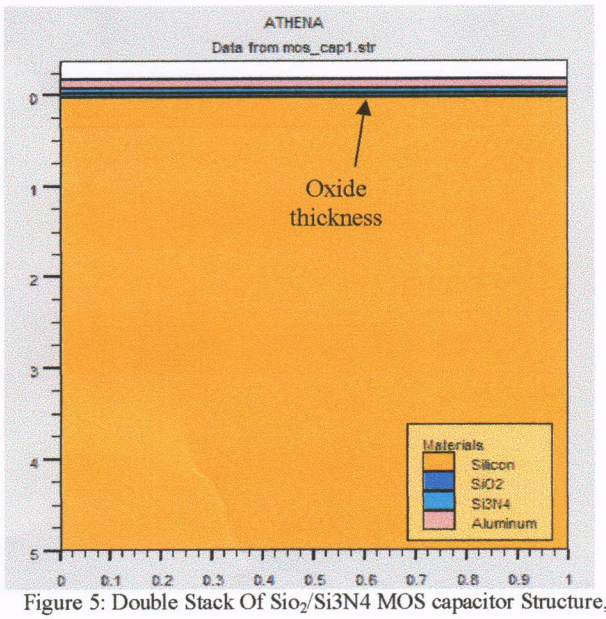

Figure 5: Double Stack Of Sio_2/Si3N4 MOS capacitor Structure, for t_{ox}=35nm

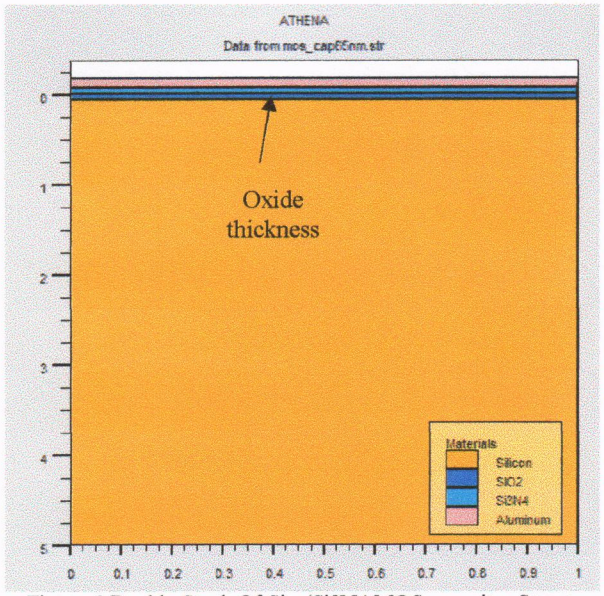

Figure 6:Double Stack Of Sio_2/Si3N4 MOS capacitor Structure, for t_{ox}=65nm

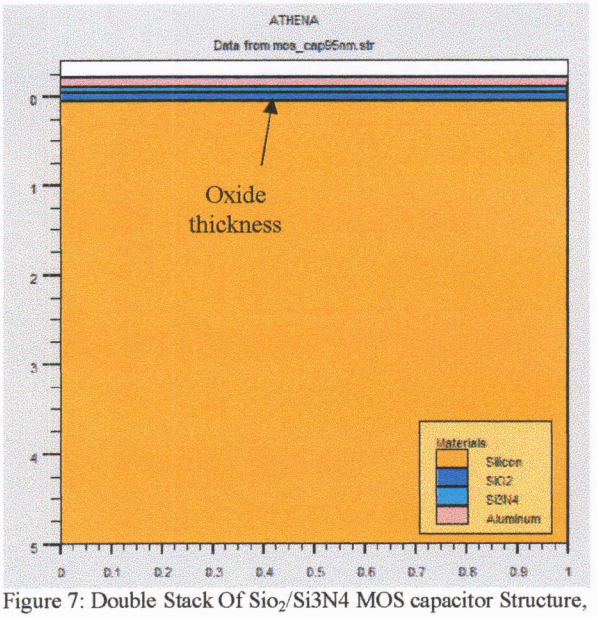

Figure 7: Double Stack Of Sio_2/Si3N4 MOS capacitor Structure, for t_{ox}=95nm

The p-type substrate for the body of MOS capacitor which is boron has been chosen with resistivity 7.5Ohms and the Silicon material is selected with <100> . Besides that, the size for this MOS capacitor structure is 1um x 5um. The simulation software must carefully define the mesh nodes at the defined regions as well as define finest meshes at high regions activity [10]. The parameters of diffuse time has been varied in order to produce the different thickness of the silicon dioxide (SiO_2) which is for 35nm, 65nm and 95nm from the simulation.

Besides that, in order to perform the sacrificial oxidation, the gate oxide thickness of 300Å before that has been extract. Then by using the extract files in ATHENA to optimized the thickness of gate oxide process, then most precise values of oxide thickness for 35nm,65nm and 95nm are shown in the output window as Table 2 shown below, where the extract statement in ATHENA simulation will run the steps of gate oxidation process. This all physical parameters are used to meet the fabricated sample of total capacitance which is C_T= $5.64x10^{-17}$F.

Diffuse Time (min)	Gate Oxide Thickness, tox (nm)
5.0	35.7169
13.2	65.2847
24.0	95.6514

Table 2: Diffuse Time Value to get Exact Value for The Gate Oxide Thickness

Next is the process of p-well implantation and p-well annealing process with implant boron dose of 1.0e12 and energy of 50kev. Then, the nitride deposition annealing process also has been done to form the layer of second gate by using Silicon Nitride SiO2N4 by set the thickness with 65nm.

```
EXTRACT> init infile="Alb06616"
EXTRACT> extract name="extract gate oxide thickness (Target thickness=950A)"
extract gate oxide thickness (T=956.514 angstroms (0.0956514 um)   X.val=0.3
EXTRACT> quit
```

Figure 8: Runtime output of extract statement

The process to deposit the aluminum layer with thickness 100nm is deposited to the top surface of the MOS Capacitor structure is using ATHENA deposit menu. Next, to perform C-V Curve, the device simulation also has been developed by using ATLAS simulator.

B. C-V Curve Characterization

In this experiment, the C-V curve characterized during the low and high frequency has been presented, in order to study the relationship between the MOS capacitor and the frequency. The gate is applied with dc bias voltage in C-V measurements, and then a low and high frequency also need to apply to obtained the capacitance at the bias voltage applied[9]. The different bias modes of an MOS capacitor considered of three different bias voltages regions such as accumulation, depletion and inversion [11].

1st Analysis: Analisis on the stack dielectric for Si02 and Si3N4 of mos cap thickness

a. Analysis the thickness of Silicon Oxide (SiO2) on MOS Capacitor

Theoretically, from the previous finding literature reports stated that decreasing the thickness of the value of dielectric tox, will leads the C_{ox} to raising up. The value of the calculated capacitance, C_{ox} has been tabulated as shown in Table 1.

Sample	T1	T2	T3
t_{ox} (nm)	35.1858	65.3741	95.0004
t_{nit}(nm)	65	65	65
Calculated C_T (F)	5.01×10^{-16}	3.48×10^{-16}	2.68×10^{-16}
Simulated C_T (F)	4.97×10^{-16}	3.46×10^{-16}	2.66×10^{-16}
% of error	0.80	0.57	0.75
% of accuracy	99.2	99.42	99.25

Table 3 : Calculated C_T by varying SiO2 thickness low frequency

i. C-V Curve for oxide thickness, tox=35nm

From the Figure 9, shown the CV Curve measurements that obtained from 1Hz of low frequency is well-illustrated. The simulation obtained were using the constant thickness of Silicon Nitride (Si3N4),t_{nit}=65nm. Besides that, at this time the thickness of Silicon Oxide SiO2 is varied.

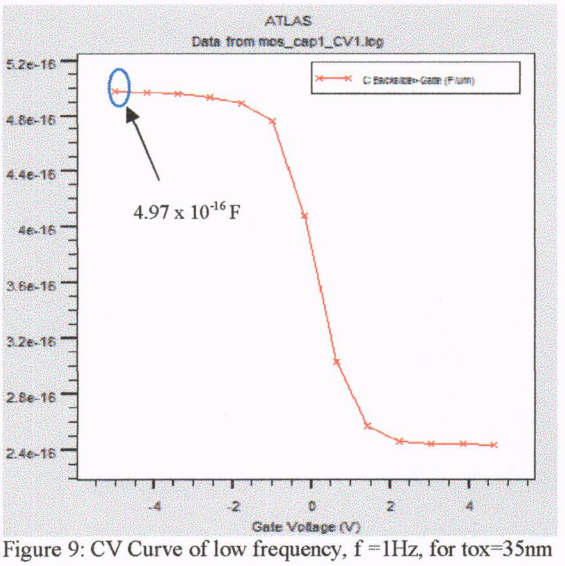

Figure 9: CV Curve of low frequency, f =1Hz, for tox=35nm

For Figure 9, the curve that obtained is well illustrated for 1Hz low frequency. When Vg is equal to 0V or less than that bias, the graph will show that range is in the accumulation regions.

ii. C-V Curve for oxide thickness, tox=65nm

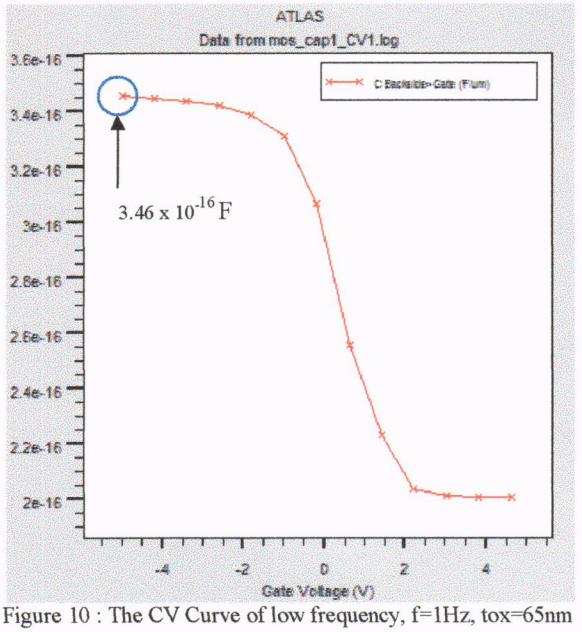

Figure 10 : The CV Curve of low frequency, f=1Hz, tox=65nm

iii. C-V Curve for oxide thickness, tox=95nm

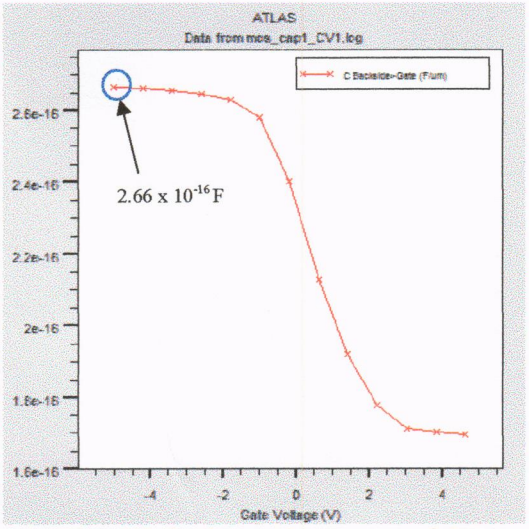

Figure 11: CV Curve of low frequency, f=1Hz, for tox=95nm

Then, the value for C_T calculated in accumulation region for t_{ox}=35nm is 5.01 x 10^{-16} F/m, then the value of C_T that calculated in accumulation region for t_{ox}= 65nm is 3.48 x 10^{-16} F/m while the value for C_T for t_{ox}= 96nm is 2.68 x 10^{-16}.

b. Analysis on stack dielectric of MOS cap by varying the Si3N4 thickness.

Sample	T1	T2	T3
t_{ox} (nm)	65	65	65
t_{nit}(nm)	35	65	95
Calculated C_T (F)	4.15 x10^{-16}	3.50 x10^{-16}	3.02 x10^{-16}
Simulated C_T (F)	4.10 x10^{-16}	3.46 x10^{-16}	2.99 x10^{-16}
% of error	1.2	1.14	0.99
% of accuracy	98.8	98.86	99.0

Table 4 : Calculated C_{ox} by varying Si3N4 thickness low frequency

For this analysis, Table 4 shown that the calculated and simulated capacitance by varying the Silicon Nitride Si3N4 and the Silicon dioxide thickness was fixed to tox =65nm. Based on the result that obtained in figure 4 , can be concluded that the lower of the thickness of silicon nitride used will results the total capacitance obtained from the MOS Capacitor.

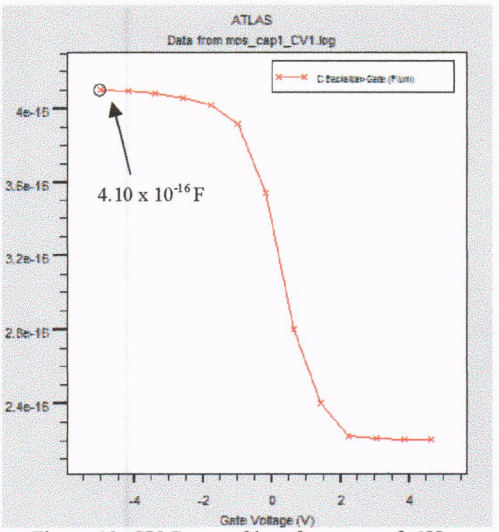

Figure 12: CV Curve of low frequency, f=1Hz, for tnit=35nm

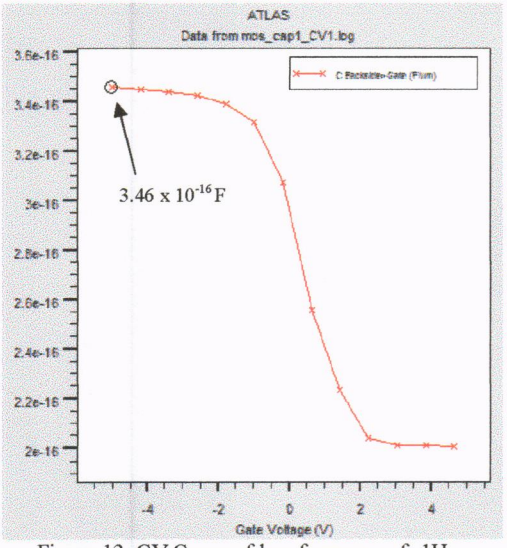

Figure 13: CV Curve of low frequency, f=1Hz, for tnit=65nm

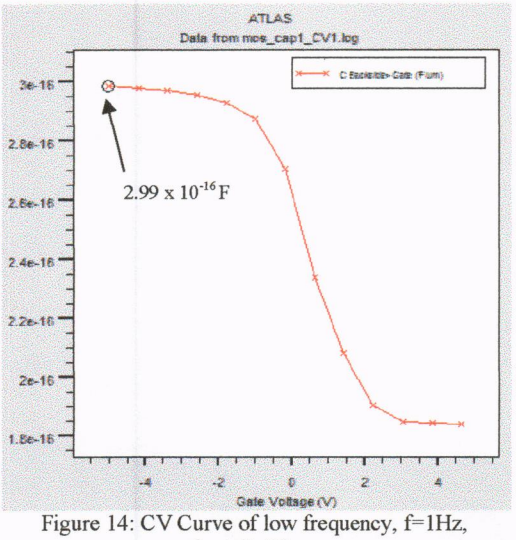

Figure 14: CV Curve of low frequency, f=1Hz, for tnit=95nm

2nd Analysis: Analysis on the permittivity of stack dielectric

For this analysis, both of the dielectric thickness has been increased to 100nm, since the result in Analysis 1 that obtained shown when the thickness reduced, will results on the simulated capacitance drastically decreased.

Sample	MIN Value	MAX Value
ε_{ox}	2	6
ε_{nit}	4	9
Calculated C_T (F)	1.18×10^{-16}	3.19×10^{-16}
Simulated C_T (F)	2.8×10^{-16}	3.14×10^{-16}
% of error	57.8	1.6
% of accuracy	42.2	98.4

Table 5 : Calculated C_{ox} by varying

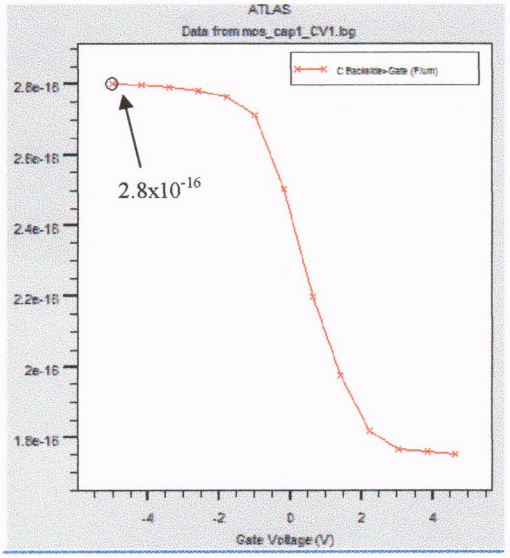

Figure 15: C-V Curve for E_{ox}=2. E_{nit} =4, for minimum value

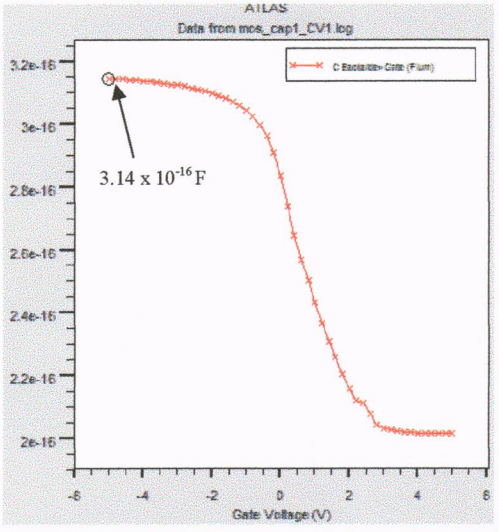

Figure 16: C-V Curve for E_{ox}=6, E_{nit} =9 for maximum value

3rd Analysis: Analysis on the area of MOS Capacitor

Then for this analysis, the area is varied to obtain the target calculated capacitance value.

Sample	A1 (um^2)	A2 (um^2)
A_{ox}	0.8	1.35
A_{nit}	0.8	1.35
Calculated C_T (F)	9.44×10^{-17}	1.59×10^{-16}
Simulated C_T (F)	9.27×10^{-16}	1.86×10^{-16}
% of error	100	16.98
% of accuracy	0	83.0

Table 6 : Calculated C_{ox} by varying

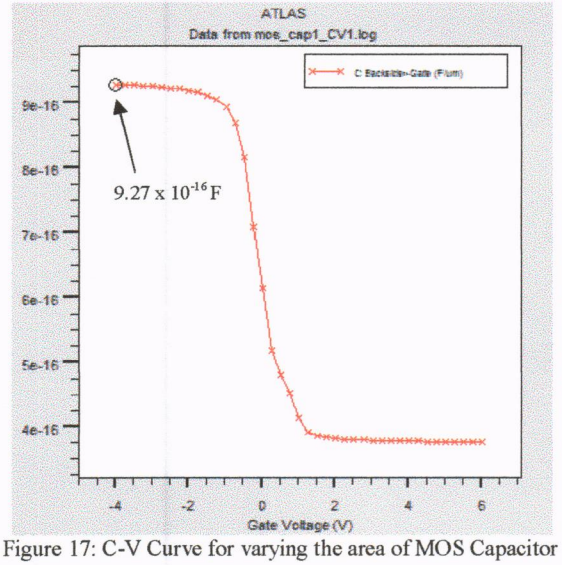

Figure 17: C-V Curve for varying the area of MOS Capacitor

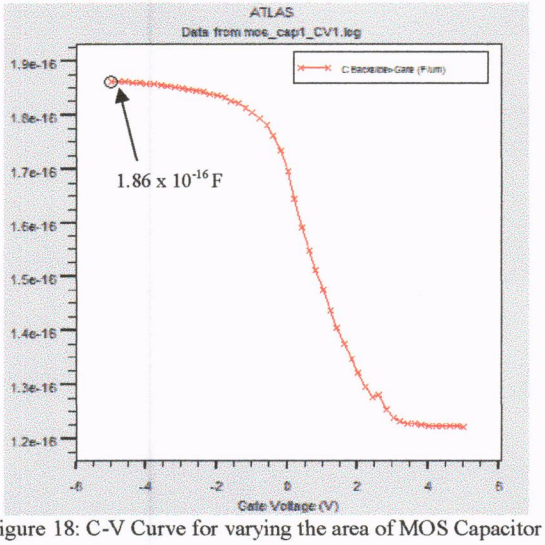

Figure 18: C-V Curve for varying the area of MOS Capacitor

4th Analysis: Analysis on all physical parameters of MOS Capacitor

ε_{ox}	$t_{ox(nm)}$	$A_{ox}(um^2)$	$t_{nit(nm)}$	ε_{nit}	$A_{ox}(um^2)$
2	100	0.75	100	4	0.75

Table 7 : Value for dielectric permittivity and thickness, also area of the MOS Capacitor

Calculated CT (F)	Simulated CT(F)	% of Error	% of accuracy
$8.85x10^{-17}$	8.1810^{-16}	100	0

Table 8: For varied all physical parameter on MOS Capacitor.

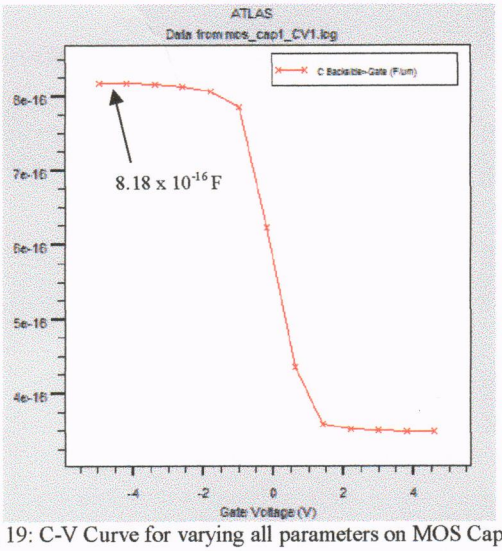

Figure 19: C-V Curve for varying all parameters on MOS Capacitor

IV. CONCLUSION

In this study, to see the both of effect on the thickness of gate oxide and the Silicon Nitride Si4Ni3 on CV Curve characteristics and also the parameters involved to analyze and those results are developed by using CV Curve measurement. It also observed that the MOS capacitance model structure in the ATHENA simulation contains few physical parameters with its measured capacitance. The correlation of important factors also involved in this experiment, such as the gate oxide and Silicon Nitride Si4Ni3 thickness, also their permittivity and the size of area for MOS capacitor structure. From all analysis that have been done, it shows that all physical parameter involved in this experiment effected the total capacitance, C_T. Since the experiment result did not completely match the measured capacitance value which is, $C_T = 5.64x10^{-17}F$, further study for this research need to fulfill the requirement for the future works. Then, in future may put few innovative way to improve the percentage of correlation between the calculated and simulation capacitance value. All this approaches that have been used also can be modified. Owing to that, material of the stack dielectric Silicon Nitride also can be replaced with another type of material.

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