DESIGN AND SIMULATION OF 65nm VERTICAL DOUBLE GATE NMOS USING SILVACO TCAD TOOLS

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ABSTRACT

This paper has demonstrated structure design and simulating electrical characteristic of Vertical Double Gate n-channel MOSFET (NMOS) using Silvaco TCAD Tools. Objectives of this study are to design 65nm Vertical NMOS, meet the specification provided by International Technology Roadmap Semiconductor (ITRS) and to study the effect threshold voltage by varying body channel doping and oxide thickness. The investigation of Vertical NMOS characteristic is done through structure design and simulation electrical characteristic using ATLAS tools Silvaco. The extracted values are compared to the ITRS specification. At gate length, Lg=65nm, channel body doping concentration of 1.5×1018 cm-3 and oxide thickness, Tox=2.2 nm, this design have a drive current of 450µA/µm, low off-state leakage at 18.14nA/µm and subthreshold swing, SubVt of 76mV/decade. From Id versus Vgs characteristic curve, threshold voltage is 0.19V at Vds=0.1V.

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CHAPTER 1

INTRODUCTION

1.1 BACKGROUND OF STUDY

Metal-Oxide-Silicon Field-Effect- Transistor (MOSFET) is increasingly used in areas as diverse as mainframe computers and power electronics. The MOSFET's long standing advantages over other types of devices are its mature fabrication technology, its successful scaling characteristics and the combination of complementary the N and P-channel MOSFETs yielding CMOS circuits. In the past twenty years, the evolution of CMOS technology has followed the path of device enhancement through downscaling for achieving density, speed, and power improvements. MOSFET scaling has been significantly propelled by the rapid advancement of lithographic techniques enabling the definition of smaller features from about 10mm in the 1960's to less than 0.1 micron meter today. During the early years of transistor scaling, Gordon Moore (in 1965) predicted that the number of transistors per square inch on integrated circuits would double every 18 months which has become known as Moore's law [1].

The recent development of strained Silicon-Germanium is a good additional tool that has made shorter channel MOSFETs attractive. Recently, fabrication of a strained Silicon-Germanium vertical channel MOSFET has been developed that does not need sophisticated lithography and whole fabrication is compatible with a standard CMOS process. CMOS devices continually scaling into the sub-100 nm regime, more complex photolithography and process technology are required to suppress roll off and drain-induced barrier lowering (DIBL) effects [2]. Since the channel length has no dependence on the critical lithography in Vertical MOSFETs, they have received much attention in sub100-nm memory and conventional logic applications [1]. These easily scalable and high-density vertical transistors are well suited for low-voltage and low-power applications. With Vertical Double Gate MOSFET, it have double of channel which giving it the potential to nearly double the processing speed of some silicon chips.