APPENDICES

5-bit Wallace-tree Thermometer-to-Binary Encoders 0.18µm CMOS Technology for Flash ADCs Comparing Conventional CMOS and Transmission Gate CMOS Full Adder

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***Abstract* – The thermometer-to-binary decoder becomes the constraint of the ultra-high speed CMOS flash analog-to-digital. This paper present two different types of 5-bit Wallace-tree thermometer-to-binary encoders for ultra-high speed in flash ADC in 1.8V, 0.18µm CMOS technology. Two different types of Wallace-tree encoders are compared using different full adder which are Conventional CMOS full adder and Transmission Gate CMOS full adder. The study is carried out to compare the parameters in these two types Wallace-tree thermometer-to-binary encoders. The parameters studied are power consumption, number of transistors, and delay.**

Keywords- Flash ADC, Wallace-tree encoder

I. INTRODUCTION

Flash analog-to-digital converter (ADC) is called as parallel ADC. Flash ADC is the fastest way to convert from analog signal to digital signal. The advantage of flash ADC is having very high sampling frequency and high conversation data rate but it has disadvantage as it requires very large chip area, low resolution and high power consumption. Flash ADC architecture uses 2^N resistors and 2^N-1 parallel comparators to convert an N-bit data. Normally flash ADC architecture 2^N-1 parallel comparators will cause high power consumption [1].

A study done by Ms.G.LMadhumati et.al [1] studied five different 5-bit thermometer-to-binary decoders which are suitable for flash analog-to-digital converter in 1.8V, 0.18µm CMOS technology. Five different designs are Wallace-tree decoder, ROM decoder, Logic-based decoder, Multiplexer-based decoder and Fat-tree decoder. Comparative study between these thermometer-to-binary decoders is done based on power consumption, count of transistors and delay. This study indicates that the combination of medium power, low transistor count, more regular structure and shorter critical path makes multiplexer-based decoder is a viable option for efficient flash ADC design.

According to a project done by Erik Säll et. al [4] which is studied about Digital decoders in flash analog-to-digital converters. The purpose of this project is to study digital decoder using a ones-counter as decoder such as Wallace-tree. Ones- counter can be fast and give global bubble error suppression. This project also suggested the improvement of the Wallace-tree decoder by applying folding. It yields decoder with less area and a circuit with shorter critical path which should make it possible to design for lower power consumption than the Wallace tree decoder.

F.Kaess et.al [3] undertook a study about a new encoding scheme for high-speed flash analog to digital converters using a Wallace tree. This study indicates that Wallace tree provide a global error filtering and its regular topology optimizes the signal propagation. Authors describe its application to a 5-bit 1.4GHz Gallium Arsenide analog-to-digital converter.

II. BACKGROUND STUDY

Flash ADC is made by cascading high speed comparator. It consists of two blocks which are comparator block and encoder block. The simplest architecture of flash ADC is shown in Figure 1 [1].

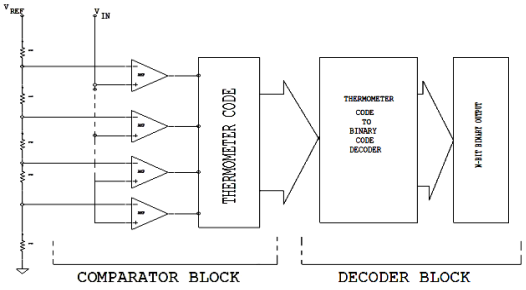

Figure 1. Simplest architecture flash ADC

For N bit converter, the circuit use 2^N-1 comparators. Flash ADC operates simultaneously comparing input signal with a resistive-divider with 2^N resistor references. The output of the comparator is high if the input voltage is high than the reference voltage at the input of the comparator. Otherwise the output is low. The point where the code change from one to zero is the point at which the input signal become smaller than the comparator reference voltage level. This is known as thermometer code encoding. In the encoder block the thermometer coded output of the comparator is converted to binary code by thermometer-to-binary encoder. Table 1 is an output binary code and the thermometer code for 5 bits.

TABLE 1. BINARY-THERMOMETER CODE IMPLEMENTATION

BINARY CODE					THERMOMETER CODE																											
A	B	C	D	E	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
0	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
0	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
0	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
0	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
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1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	0	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

Normally the characteristic of the thermometer-to-binary encoder limit the overall performance of flash ADC.

III. METHODOLOGY

The flow chart in Figure 2 indicates the step to design 5-bit Wallace-tree thermometer-to-binary encoders in 1.8V, 0.18um CMOS technology comparing Conventional CMOS full adder and Transmission Gate CMOS full adder.

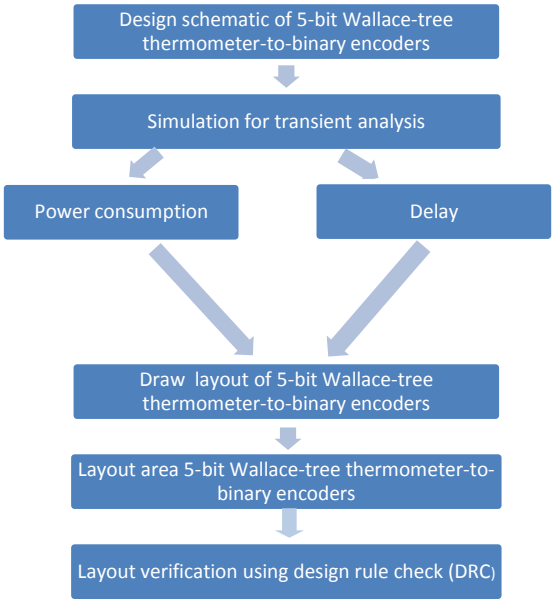


Figure 2. Flow chart of the project

Schematic two different types of Wallace-tree encoders that compared using different full adder which are Conventional CMOS full adder and Transmission Gate CMOS full adder are draw in GATEWAY Silvaco tool. The number of transistors is counted from the schematic. Simulation of transient analysis is done to obtained power consumption and transient analysis. The data collected are analyzed based on three parameters to compare the performance of both encoders. The parameters are power consumption, number of transistors and delay. Layout of these two encoders is draw using EXPERT Silvaco tool and design rule check is done for layout verification.

IV. WALLACE-TREE ENCODER FOR FLASH ADC

Wallace-tree encoder contains a tree of full adders. It takes the output of the comparator block directly and processes it [1]. It's simply count the number of ones appeared as its inputs and encodes them into binary code. Wallace –tree encoder is one of ones-counter topology. The ones-counter technique gives global bubble error correction or suppression [3] [4]. Another advantage of the ones-counter is depending on the speed requirement on the ADC and suitable ones-counter topology may be selected by trading speed for power. Figure 3 shows a 5 bit Wallace-tree encoder flash ADC.

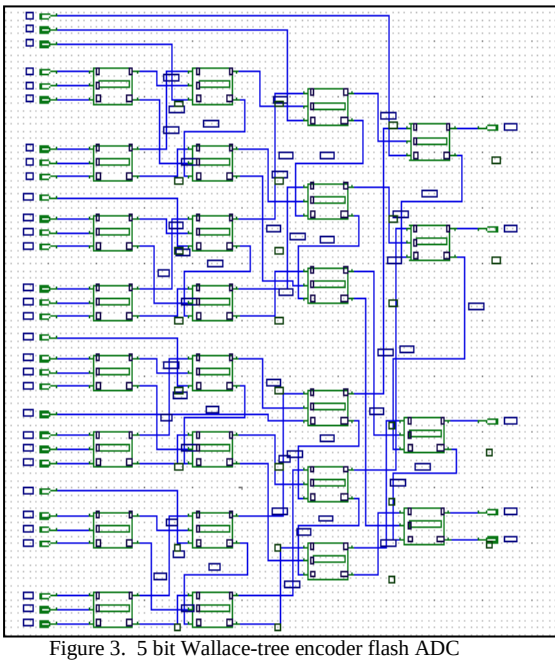


Figure 3. 5 bit Wallace-tree encoder flash ADC

V. FULL ADDERS FOR WALLACE-TREE FOR FLASH ADC

Full adder cell design in Wallace-tree thermometer-to-binary encoder for flash ADC is used to convert the thermometer coded output of the comparator to binary code can be implemented by various approaches. This part presented two designs of full adder that used in this paper. The two designs are Conventional CMOS Full Adder and Transmission Gate CMOS Full Adder. Conventional CMOS full adder has 28 transistors in one full adder cell where Transmission Gate CMOS full adder uses 20 transistors.

A. Conventional CMOS Full Adder

Conventional CMOS full adder cell is category as one of static logic. Static logic is the best type for low power circuit design because it eliminates precharging and decrease extra power dissipation [7]. Conventional CMOS full adder cell has 28 transistors and based on regular CMOS structure which contains pull-up and pull down networks [5]. The advantage of Conventional CMOS full adder is high noise margin and suitable for operation at low voltage and small mobility ratio for transistor sizes. However, Conventional CMOS full adder produces an unwanted additional delay and larger silicon area [7]. Structure of Conventional CMOS full adder is illustrated in Figure 4.

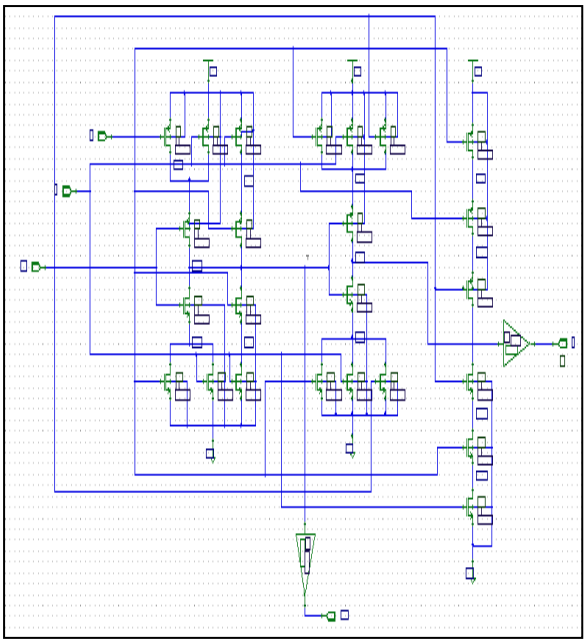


Figure 4. Conventional CMOS full adder

B. *Transmission Gate CMOS Full Adder*

Transmission gate CMOS full adder cell is based on transmission gate and has 20 transistors [5] [7]. Transmission gate logic circuit is a special type of pass-transistor logic circuit [6]. At the same power dissipation it shows the better speed than the CMOS full adder [7]. The main disadvantage of transmission gate is it requires double number of transistors than pass transistor logic or it implements the same circuit. Figure 5 indicates Transmission gate CMOS full adder.

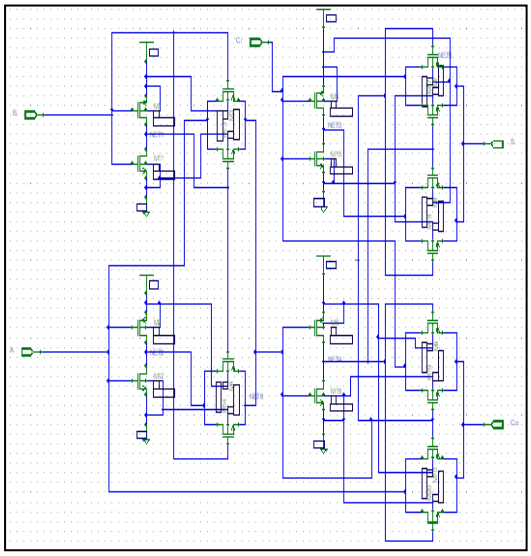


Figure 5. Transmission gate CMOS full adder

VI. RESULT AND DISCUSSION

All the simulation have been done using Silvaco tool. The schematics are drawn using GATEWAY Silvaco tool with 0.18µm CMOS technology and with 1.8V supply voltage. Transient analysis was applied to obtain power consumption and delay. The number of transistor count calculation is carried out for 5-bit Wallace-tree thermometer-to-binary encoders. Table 2 illustrates the details of simulation results for two different types of 5-bit Wallace-tree thermometer-to-binary encoders based on three parameters. The parameters are power consumption, number of transistors and delay. The results of power consumption, number of transistors, and delay for two different 5-bit Wallace-tree encoders are illustrated in Table 2.

TABLE 2. SIMULATION RESULTS OF TWO DESIGNS 5-BITS WALLACE_TREE THERMOMETER-TO-BINARY ENCODERS

No	**Full Adder Type**	**Power Consumption**	**Number of transistors**	**Delay**	**Technology**
1	Conventional CMOS Full Adder	4.27403e-004	616	360.7ps	0.18µm
2	Transmission Gate CMOS Full Adder	6.82652e-004	440	834.15 ps	0.18µm

A. *Power Consumption*

Power consumption depends on the application, the kind of circuit implemented and the design technique used. Power consumption can be reduced by lowering the supply voltage [6]. Power consumption of full adder can be measured using equation (1).

$$P_{total} = P_{switching} + P_{short\text{-}circuit} + P_{leakage} \quad (1)$$

The comparison of power consumption between present study and previous study which is done by Ms.G.L.Madhumati et.al is illustrated in Table 3 and is plotted in Figure 6.

TABLE 3. COMPARISON RESULT BETWEEN PRESENT STUDY AND PREVIOUS STUDY BASED ON POWER CONSUMPTION

Parameter	**Case Study**		
	Present Study		**Previous Study Wallace tree**
	Conventional CMOS Full Adder	***Transmission Gate CMOS Full Adder***	
Power Consumption	$4.27403e^{-004}$	$6.82652e^{-004}$	$7.9021e^{-004}$

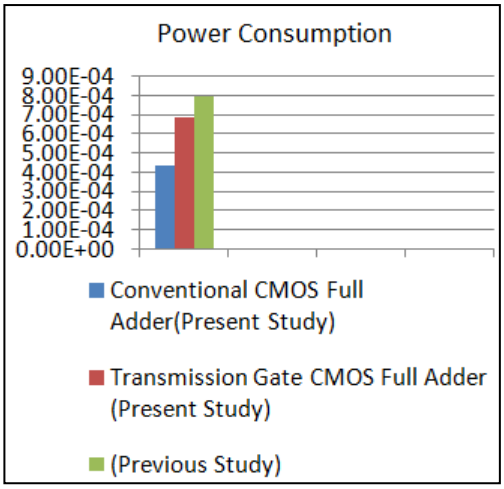


Figure 6. Power consumption versus 5-bit Wallace-tree thermometer-to-binary encoders between present study and previous study

Based on power consumption in Table 3, both power consumption for Wallace-tree of present study which use Conventional CMOS full adder and Transmission Gate CMOS full adder is lower than power consumption of previous study. Wallace-tree encoder that used Conventional CMOS full adder consumes lowest power compared to Transmission Gate CMOS full adder and previous study.

B. Number of Transistors

Number of transistors used for two designs 5-bit thermometer-to-binary encoders are showed in Table 4. Graph of Figure 7 represents number transistors for these two encoders.

TABLE 4. NUMBER OF TRANSISTORS FOR TWO DESIGNS 5-BIT THERMOMETER-TO-BINARY ENCODERS

Parameter	Conventional CMOS Full Adder	Transmission Gate CMOS Full Adder
Number of Transistors	616	440

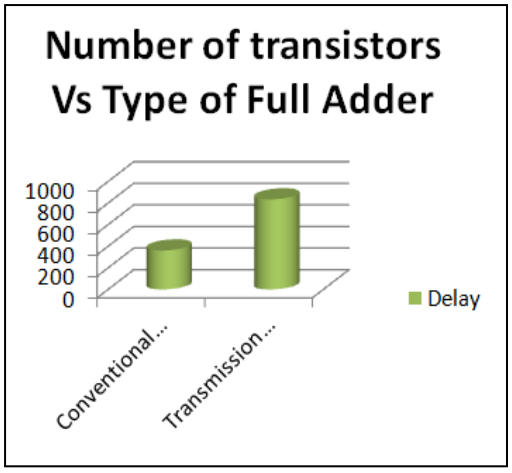


Figure 7. Number of transistors versus type of full adder for two 5-bit Wallace-tree thermometer-to-binary encoders

According to Table 4 and Figure 7, Wallace-tree encoder that used Transmission Gate CMOS full adder required less number of transistors compared to Wallace-tree encoder that used Conventional CMOS full adder.

C. Delay

The circuit propagation delay is determined by number of inversion levels, the number of transistors in series and transistor sizes. Delay between Wallace-tree encoder that used Conventional CMOS full adder and Transmission Gate CMOS full are presented in Table 5. Figure 8 indicates delay that produced from these two Wallace-tree encoders.

TABLE 5. DELAY FOR TWO TYPES 5-BIT THERMOMETER-TO-BINARY ENCODERS

Parameter	Conventional CMOS Full Adder	Transmission Gate CMOS Full Adder
Delay	360.7ps	834.15ps

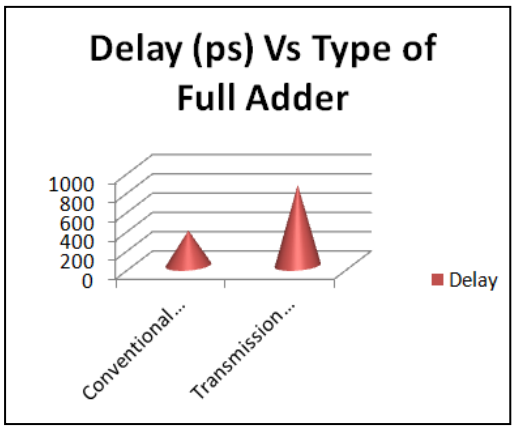
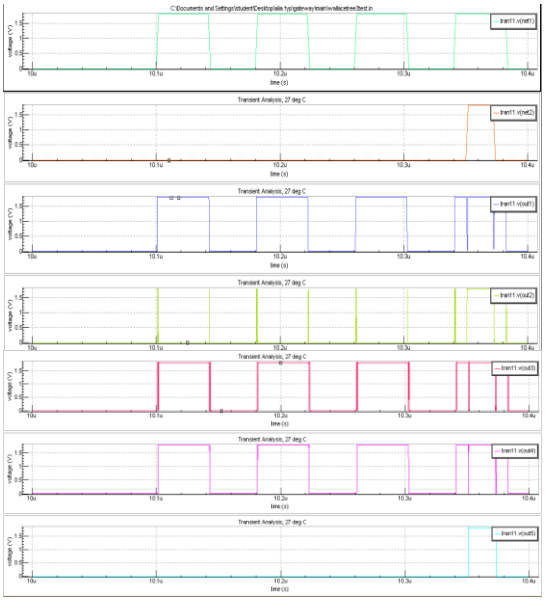


Figure 8. Delay in unit ps versus type of full adder for two designs 5-bit Wallace-tree thermometer-to-binary encoder

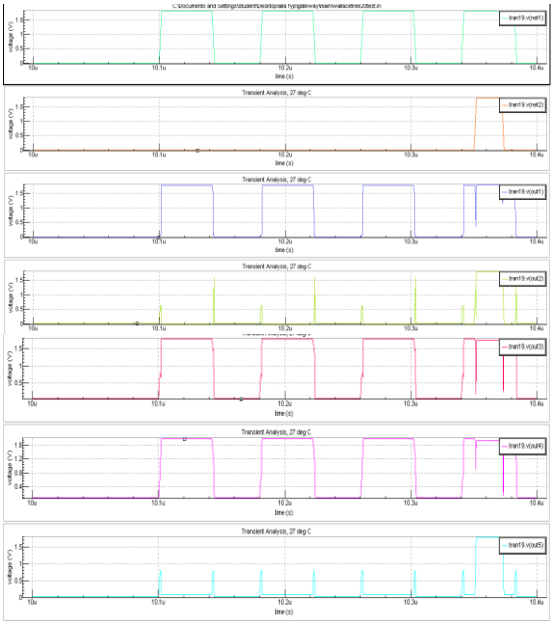
From the result obtained between Wallace-tree thermometer-to-binary encoder that used Conventional CMOS full adder and Transmission Gate CMOS full adder it shows Wallace-tree that used Conventional CMOS full adder produced lower delay.

D. Transient Analysis

Figure 9 represents transient analysis for two designs of 5-bit thermometer-to-binary encoders when inputs are injected between input 19 to inputs 31.



(A) Conventional CMOS Full Adder



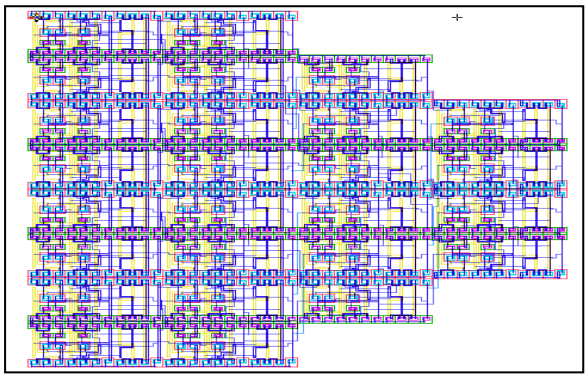
(B) Transmission Gate CMOS Full Adder

Figure 9. Transient analysis for two different designs of 5-bit Wallace-tree thermometer-to-binary encoders.

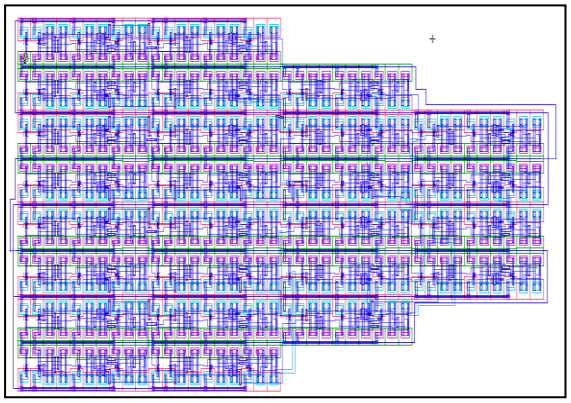
Based on transient analysis for two different designs of 5-bit Wallace-tree thermometer-to-binary encoders in Figure 9, it shows that the transient analysis is followed binary-thermometer code implementation and get as expected as truth table in Table 1.

E. Layout

EXPERT Silvaco tool is used to draw the layout of thermometer-to-binary encoders. Figure 10 illustrates the layout of two designs 5-bit Wallace-tree thermometer-to-binary encoders.



(A) Conventional CMOS Full Adder



(B) Transmission Gate CMOS Full Adder

Figure 10. Layout for two types 5-bit Wallace-tree thermometer-to-binary encoders

Table 6 represents layout area for two designs 5-bit Wallace-tree thermometer-to-binary encoders.

TABLE 6. LAYOUT AREA OF TWO DESIGNS 5-BITS WALLACE-TREE THERMOMETER-TO-BINARY ENCODERS

Parameter	Conventional CMOS Full Adder	Transmission Gate CMOS Full Adder
Layout area	19633.96µm^2	8141.92 µm^2

According to Table 6, Wallace-tree encoders that used Transmission Gate CMOS full adder required smaller area compared to Conventional CMOS full adder.

VII. CONCLUSION

This paper has studied design and simulation of two different designs 5-bit Wallace-tree thermometer-to-binary encoders. These two design encoders are compared using different full adder which are Conventional CMOS full adder and Transmission Gate CMOS full adder. Three parameters have been carried out to compare between these two encoders. The parameters are power consumption, number of transistors and delay. From the results obtained, it can be concluded that Conventional CMOS full adder and Transmission Gate CMOS full adder yield lower power consumption compared to the previous work. In addition, Conventional CMOS full adder consumes lower power consumption than Transmission Gate CMOS full adder. However, it requires more transistors and large area. Besides that, Conventional CMOS full adder generates lower delay. The combination of power consumption, number of transistors and delay makes Conventional CMOS Full Adder is suitable full adder to use in Wallace-tree thermometer-to-binary encoder for efficient flash ADC designs.

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