TRANSLATION BUFFER DESIGN PROJECT

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In the name of Allah The Most Gracious and The Most Merciful

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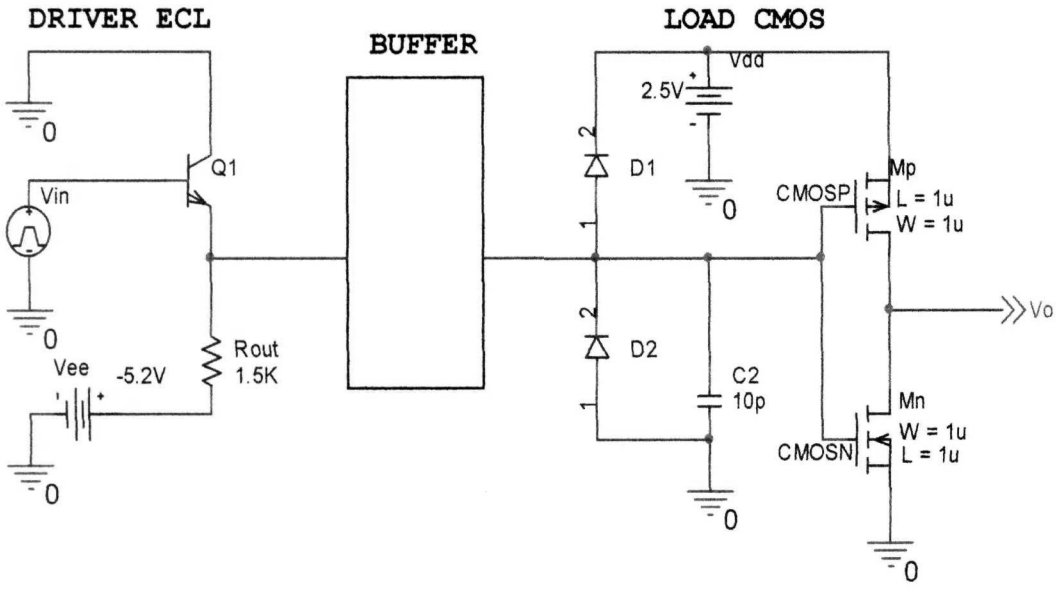
ABSTRACT

Translation buffers are used in common everyday applications to convert properties of different logic types to be compatible with other logic types.

This project is to design a translation buffer using the CMOS process that allows a 100K ECL logic block to drive 1.5 CMOS chip. A common design tool Pspice was used to analyze the buffer to produce the required specification.

The design translation buffer will be used to fit the schematic below containing the driver ECL and load CMOS.



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INTRODUCTION

1.1 Introduction

The goal of this project is to design a buffer that provides an interface between ECL circuits and CMOS circuit.

Translation buffer are used commonly everyday application to convert properties of different logic types to be compatible with other logic types. For this project, the translation buffer is designed to allow 100K ECL logic block to drive 1.5V CMOS chip.

The objectives of this project is to investigate ratio W/L of CMOS if varies to rise and fall time and analyze the propagation delay of the translation buffer circuit. Certain important characteristics are desired to design translation buffer circuit to achieve high reliability of operation and good balance among performance characteristics.

For this project, an output buffer amplitude levels should be regenerated in passing from the input to the output of a circuit. This requirement apply a voltage transfer characteristic in the general shape as shown in figure 1.