5-BIT WALLACE-TREE THERMOMETER-TO-BINARY ENCODERS 0.18μm CMOS TECHNOLOGY FOR FLASH ADCs COMPARING CONVENTIONAL CMOS AND TRANSMISSION GATE CMOS FULL ADDER

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ABSTRACT

The thermometer-to-binary decoder becomes the constraint of the ultra-high speed CMOS flash analog-to-digital. This paper present two different types of 5-bit Wallace-tree thermometer-to-binary encoders for ultra-high speed in flash ADC in 1.8V, 0.18µm CMOS technology. Two different types of Wallace-tree encoders are compared using different full adder which are Conventional CMOS full adder and Transmission Gate CMOS full adder. The study was carried out on these two types Wallace-tree thermometer-to-binary encoders in term of its parameters, namely power consumption, number of transistors, and delay. In this project, the simulation results are generated using SILVACO EDA tool. Gateway Silvaco EDA tool is used in the design and the schematic simulation. Layout and verification of the design was verified using Expert SILVACO EDA tool. The results showed that the proposed study produces better performance in power consumption over the previous work. The power consumption for the encoder using Conventional CMOS full adder reads $4.27403e^{-004}$W while for the Transmission gate CMOS full adder reads $6.82652e^{-004}$W. In addition, according to the results, encoder using Conventional CMOS full adder can be concluded to be a suitable full adder to be used in Wallace tree thermometer-to-binary encoder for efficient flash ADC designs based on power consumption, number of transistors used and delay. Encoder using Conventional CMOS full adder consume $4.27403e^{-004}$W power consumption and 360.7ps delay but requires 616 number of transistors.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

This thesis presents two designs of 5-bit Wallace-tree thermometer-to-binary encoders for flash ADC using two different full adder cells. Two types of full adders are Conventional CMOS and Transmission Gate CMOS full adders. Thermometer-to-binary encoder in Flash ADC is used to convert the output of comparator which is thermometer code to binary code. The objective of this project is to design the schematic and analyze 5-bit Wallace tree thermometer-to-binary encoders. The design used 0.18µm CMOS technology and 1.8V. The parameters studied were power consumption, number of transistors used and the delay time. Thermometer-to-binary encoders become the constraint of the ultra-high speed CMOS flash ADC. Thermometer-to-binary encoders can have significant effect on the overall flash ADC performance.

This paper will compared the simulation result from previous research about comparison of 5-bit thermometer-to-binary decoders in 1.8V, 0.18µm CMOS technology for flash ADCs which was done by Ms. G.L Madhumati [1]. The comparison between present work and previous work is based on power consumption. Besides that, the comparison of Wallace-tree encoders using different full adder cells for present work are in term of power consumption, number of transistors used and the delay time.