Comparative Study on 90nm CMOS SRAM Sense Amplifiers

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***Abstract* - This paper will investigate the sensing delay optimization and power consumption of each sense amplifier. The optimization will apply multi-Vth or MTCMOS techniques for better sensing delay, with the critical path transistors will use low-Vth model. The initial optimization is done by calculating for the most proper transistor sizing in term of sensing delay and power. The result obtained shows MTCMOS design improves sensing delay in term of smaller bit-lines difference *(ΔBL)* required for full-swing amplification as compared to single std-Vth. MTCMOS design also improves total power consumption at least 12% reduction as compared to single std-Vth design. The selected sense amplifier circuits to be simulated are Current Sense Amplifier (CSA), Charge-Transfer Sense Amplifier (CTSA), and High-Speed Sense Amplifier (HSSA). The SRAM used is basic 6T SRAM for general purpose only.**

Keyword - sense amplifier (sa), 90nm technology, current sa, charge transfer sa, high speed sa, MTCMOS.

I. INTRODUCTION

SRAM stand for Static Random Access Memory, a non-volatile memory that remains the content as long as the power is supplied. The sense amplifier operates only during read into memory phase.

Sense amplifier (SA) is used to detect the very small difference voltage at bit-lines and amplify the signals to its full-digital voltage swing before the signals are fully charged or discharged. This situation causes the time taken to read the content of memory is shorten since the circuitry does not requires to wait until the signals getting fully charged or discharged to determine either it is '1' or '0'. The small spark or glitch at both bit-lines may determine its state. So the memory may take it quickly either as '1' or '0' rather than trying to calculate or wait for its voltage full swing level, thus saves time in read operation into memory.

The selected sense amplifiers studied in this paper are the modified circuit from the original ones. CSA [1] is modified circuit from High-Speed Clamped Bit-line Current Mode Sense Amplifier [3]. HSSA [2] is based from Conventional Current Sense Amplifier [2]. While CTSA [1] applies the charges distribution from high bit-line capacitance to the lower capacitance of sense amplifier outputs nodes [1].

This paper is organized as follow: Section II will discuss about the parameter that being investigated which is *ΔBL*, sensing delay and power consumption. Section III, IV and V will discuss about the operation of CSA, CTSA and HSSA respectively. Section VI will discuss about simulation result and Section VII will conclude the result as well as recommendation for better performance and result.

II. METHODOLOGY

The scope of study in this paper includes sensing delay, bit-lines differential signal *ΔBL*, threshold voltage and power supply, VDD.

Sensing delay in sense amplifier refers to the time taken for bit-lines generates just enough difference signal to determine its full swing at output nodes, before the bit-lines completely discharged. In Fig. 2 shows the example timing scheme of sense amplifier. Sensing delay is associated with *ΔBL* since sense amplifier required certain period to distinguish the noise when the bit-lines has not generate enough differential signals.

The second parameter is Vth. Threshold voltage is the minimum bias required to create channel but not ready to conduct current yet. Smaller Vth required shorter time to develop channel and smaller gate bias swing. Therefore the transistor may be turned ON early and reach or enter to the saturation level. We minimize the scope only for critical path which is the cross-coupled inverter part and differential amplifier part in HSSA. The rest which is non-critical path will use standard-Vth model [5].

The third parameter is VDD. Other than shrinking the technology size that forces to lower VDD to be applied, the capability of an IC to tolerate with multi level power supply is a powerful advantage. Advance IC such as microcontroller has special features which is low power protection circuitry that allows keeping function even with low power supply without corrupting any data stored inside it. So, by varying the power supply, it means the sense amplifiers in this paper are ready and able to tolerate with such voltage drop circumstance and remain its full performance.

Fig.1 shows the basic operation flow of sense amplifier.

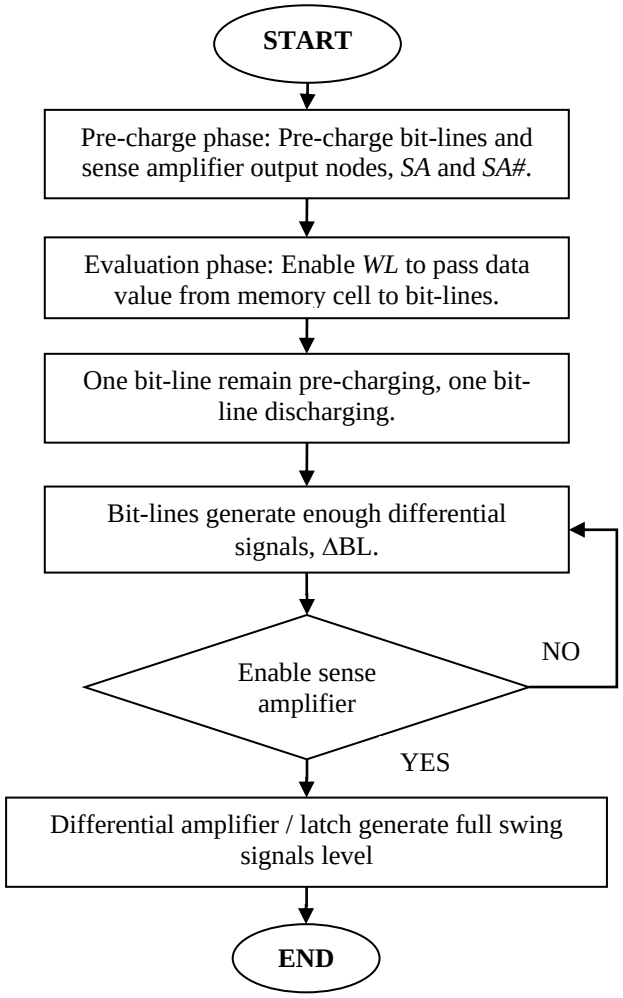

Figure 1: The Operation of Sense Amplifier.

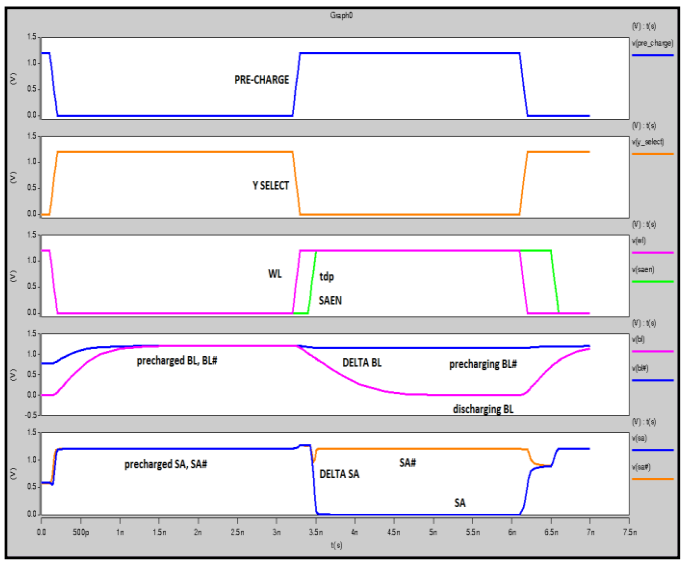

Figure 2: Example of bit-lines differential signal measurement

III. Current Sense Amplifier

The operation of CSA [1] in Fig. 3 will be such these: Initially, the bitlines (*BL* and *BL#*) and SA output (*SA* and *SA#*) will be pre-charged to *VDD* by setting up *Pre-charge* to *VSS* and *Yselect* to *VDD*. Output nodes *SA* and *SA#* are initially pre-charged high before generates a full swing differential signal once the *SAEN* is enabled to sense the *ΔBL*.

During Evaluation phase, *Pre-charge* is set to *VDD* and *Yselect* is set to *VSS* causes the bit-lines signals to be transferred from the selected memory cell to sense amplifier. By enabling the sense amplifier, the differential voltage will be measured between *SA* and *SA#*. This differential input then will be used as reference for the next digital usage in memory. The two inverters at *MN14* are used as delay of *SAEN*.

M10 and *M11* are used to isolate bit-lines from sense amplifier output nodes for better signals recognition and amplification.

M8 – M14 later will be set for different design in MTCMOS. *M8 – M14* formed a cross-coupled latch, make it as critical path in CSA. Thus they will use lower Vth compared to non-critical path.

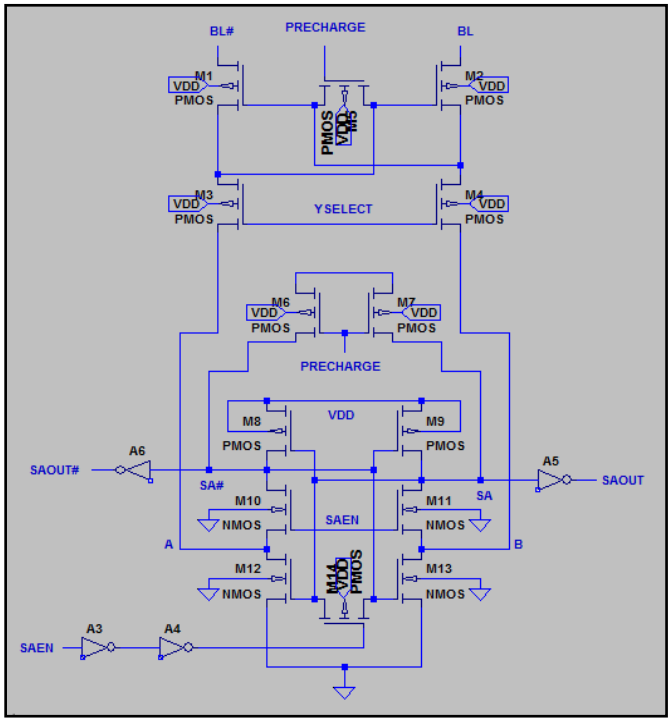

Figure 3: Current Sense Amplifier.

IV. Charge Transfer Sense Amplifier

The operation of CTSA [1] in Fig. 4 will be such these: The operation on CTSA is based on charged redistribution from high bit-lines capacitance to the low capacitance at the sense amplifier output nodes *SA* and *SA#* [1]. During Pre-charge phase, bit-lines (*BL, BL#)* and *Yselect* are pulled high to *VDD* while *Pre-charge* is pulled down to *VSS*. With enable *SAEN* is

set to high, sense amplifier output nodes (*SA, SA#*) are pre-discharged to *VSS*.

During Evaluation phase, *Yselect* is pulled down and *Pre-charge* is pulled up. Data signals from the selected memory cell will be transferred to sense amplifier. CTSA is enabled by setting *SAEN* to low, pass through bit-lines signal to the sense amplifier and differentiate the small difference between these signals.

M9 – M12 forms an inverter that being used to isolate the bit-lines and sense amplifier during pre-charge and sensing phase for better signals recognition and amplification.

M13 – M17 later will be set to low-Vth model in MTCMOS design. The *M13 – M17* are the critical path in CTSA.

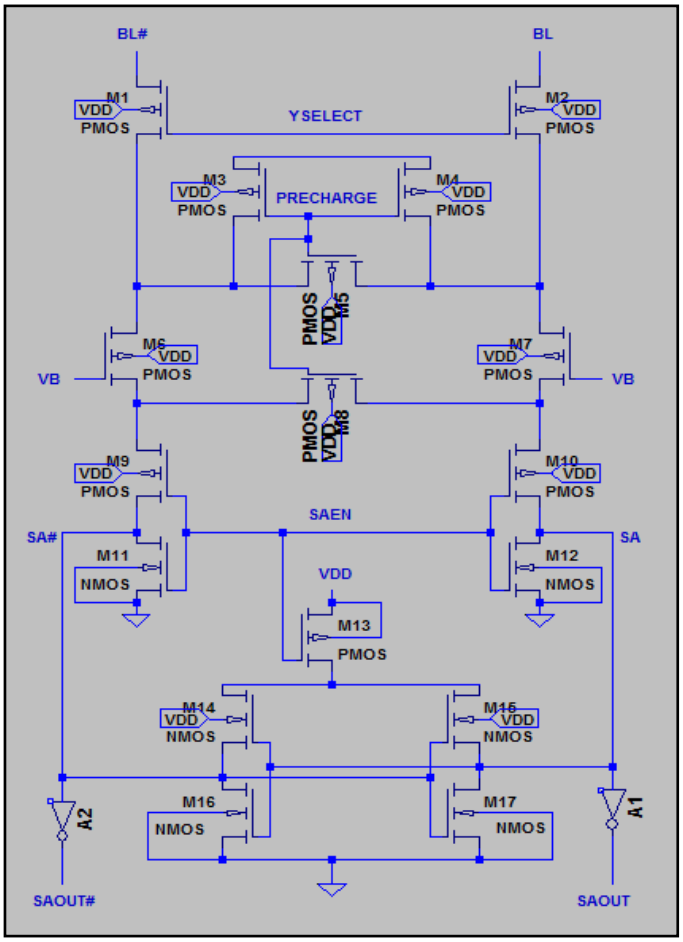

Figure 4: Charge Transfer Sense Amplifier

V. High Speed Sense Amplifier

The operation of HSSA [2] in Fig. 5 will be such these: In pre-charge phase, sensing enable *SAEN* is pulled down to *VSS*. This causes the *OUT#* and *OUT* will be set to *VDD*.

In sensing mode, *SAEN* is pulled high to *VDD*. Pre-charging output nodes will be stopped since transistors *M1* and *M6* are turned off. *M7* and *M8* from switching circuit formed in inverter circuit will pass the bit-lines signal to the differential amplifier formed by *M9 – M11*. Both *BL* and *BL#* signals will be compared using current-mirror circuit formed by *M2 – M5* for *OUT* and *OUT#* full swing level.

Switching circuit that consists of *M7, M8, M13* and *M14* are used to isolate between sense amplifier output nodes and bit-lines, for better signals recognition and amplification.

In MTCMOS design, *M2 – M5* and *M9 – M12* will be using low-Vth model in multi-Vth design.

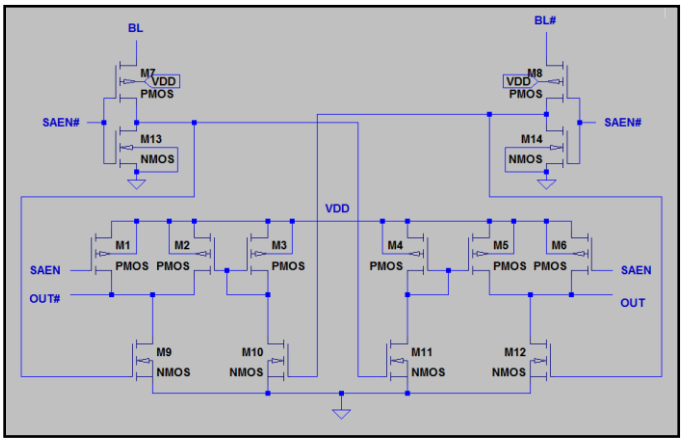

Figure 5: High Speed Sense Amplifier

VI. Simulation Result

A. Bit-lines differential voltage level

Fig. 2 shows the example of bit-lines differential signal measurement during read 0 of CSA using std-Vth model. Initially, both bit-lines (*BL, BL#*) are pre-charged, and SRAM hold the memory *Q* equal to 0 and *Q#* is 1. Then word line *WL* will be pulled high to pass the *Q* and *Q#* inside SRAM cell into *BL* and *BL#*. Immediately just after *WL* is pulled high, *BL#* will maintain pre-charged while *BL* will discharge. The small discharging on *BL#* (*ΔBL*) then will be sensed to determine its full swing level before it completely discharged.

Proper sensing enable is critical. If sense amplifier enabled too early, bit-lines may not generate enough differential signal yet, thus the correct data will not being sensed and forwarded for the next digital usage [7]. If the sense amplifier enabled too late, the SRAM is too slow and less efficient since it need very large swing level [7].

In Fig. 2, the sense amplifier enable *SAEN* is intentionally triggered with some delay after *WL* is pulled high. This is for allowing bit-lines to develop enough voltage difference so that the correct data can be sensed. Then the sense amplifier output, *SA* and *SA#* will generate full swing complementary signals to each other before the *BL#* completely discharging. *SAEN* delay obtained using Eq. 1 below:

$$t_{PD} = \left(\frac{C_{BL}}{I_{READ}}\right)\Delta v \qquad (1)$$

C_{BL} is the bit-lines capacitance, I_{READ} is the current drawn during read operation and ΔV is the voltage difference of bit-lines.

Table 1 and Table 2 shows the difference bit-lines signals required to be amplified to its full swing for CSA. The data shows that CSA design with MTCMOS model can amplify the small bit-line signals faster than single std-Vth model.

MTCMOS model can be amplified about 90% of VDD at least after 100ps delay between *WL* and *SAEN* with ΔBL about 0.16V. Compared to single std-Vth model, full swing voltage level can be reached to about +/-87% of VDD after 150ps delay with ΔBL 0.21V. So, by applying MTCMOS design may increase speed in detecting bit-lines difference thus full swing voltage level may be generated quickly.

Table 1: Bit-lines differential signal of CSA during read 1

CSA, 1.20 VDD, Read 1				
tpd(s)	Average ΔI_{read} (A)	Average ΔBL (V)	ΔSA	
			Std-Vth (V)	MTCMOS (V)
50p	0.0033	0.10	0.7734	0.8475
100p	0.0032	0.16	0.9924	1.0945
150p	0.0032	0.21	1.0535	1.1119
200p	0.0032	0.26	1.0413	1.1060

Table 2: Bit-lines differential signal of CSA during read 0

CSA, 1.20 VDD, Read 0				
tpd(s)	Average ΔI_{read} (A)	Average ΔBL (V)	ΔSA	
			Std-Vth (V)	MTCMOS (V)
50p	0.0033	0.10	0.7861	0.8897
100p	0.0032	0.16	0.9925	1.0717
150p	0.0032	0.21	1.0528	1.0952
200p	0.0032	0.26	1.0424	1.1222

Table 3 and Table 4 shows the difference bit-lines signals required to be amplified to its full swing for CTSA. MTCMOS model shows that with the same ΔBL about 0.24V, signals amplification can reach about 90% of VDD after 150ps delay as compared to single std-Vth after 200ps delay.

Table 3: Bit-lines differential signal of CTSA during read 1

CTSA, 1.20 VDD, Read 1			
tpd(s)	Average ΔBL (V)	SA	
		Std-Vth (V)	MTCMOS (V)
50p	0.11	0.8269	0.8340
100p	0.18	0.9529	0.9659
150p	0.24	0.9969	1.0442
200p	0.30	1.0266	1.0556

Table 4: Bit-lines differential signal of CTSA during read 0

CTSA, 1.20 VDD, Read 0			
tpd(s)	Average ΔBL (V)	SA#	
		Std-Vth (V)	MTCMOS (V)
50p	0.11	0.8083	0.8347
100p	0.18	0.9605	0.9661
150p	0.24	0.9982	1.0443
200p	0.30	1.0256	1.0544

Table 5 and Table 6 shows the difference bit-lines signals required to be amplified to its full swing for HSSA. The data shows that HSSA required large bit-lines difference ΔBL compared to CSA and CTSA even though *SAEN* is triggered with same delay. HSSA has to wait until 0.8V ΔBL generated for full swing amplification, causes to higher power consumption and low speed.

Table 5: Bit-lines differential signal of HSSA during read 1

HSSA, 1.20 VDD, Read 1			
tpd(s)	Average ΔBL (V)	ΔSA	
		Std-Vth (V)	Low-Vth (V)
50p	0.80	1.0659	1.0601
100p	0.87	1.1331	1.0635
150p	0.88	1.1317	1.0627
200p	0.89	1.1343	1.0702

Table 6: Bit-lines differential signal of HSSA during read 0

HSSA, 1.20 VDD, Read 0			
tpd(s)	Average ΔBL (V)	ΔSA	
		Std-Vth (V)	MTCMOS (V)
50p	0.80	1.1234	1.0601
100p	0.87	1.1331	1.0635
150p	0.88	1.1249	1.0670
200p	0.89	1.1343	1.0702

B. Total power consumption

Table 7 summarized the total power consumption for each sense amplifier with different VDD during both read 0 and read 1 cycle. The data shows that CTSA consumed less power compared to CSA and HSSA consumed largest power among the three sense amplifiers.

The aim of varying VDD is to investigate which sense amplifier consumes more power, so that we may pre-determine its proper applications. For example, if low power is the top priority for battery-run device then speed can be traded-off for slower. So CTSA may suitable for this kind of application. For high speed application, CSA may be the better choice since CSA offers fast sensing delay with low power. HSSA may be suitable for low speed with high power.

Table 7: Total power consumption with different vdd during Read 0

SA	VDD (V)	Ptotal (mW) Read 0		
		Std-Vth	MTCMOS	% Reduction
CSA	1.08	-1.7762	-0.8000	54.96
	1.20	-2.0107	-1.0102	49.76
	1.32	-4.0798	-1.2493	69.38
CTSA	1.08	-1.7157	-0.7530	56.11
	1.20	-2.6485	-0.9684	63.44
	1.32	-3.9372	-1.1234	71.47
HSSA	1.08	-1.8633	-1.5899	14.67
	1.20	-2.4168	-2.1085	12.76
	1.32	-3.0968	-2.7093	12.51

Table 8: Total power consumption with different vdd during Read 1

SA	VDD (V)	Ptotal (mW) Read 1		
		Std-Vth	MTCMOS	% Reduction
CSA	1.08	-1.5760	-0.6000	61.93
	1.20	-2.7454	-1.0105	63.19
	1.32	-4.0801	-1.2496	69.37
CTSA	1.08	-1.7245	-0.7530	56.34
	1.20	-2.3914	-0.9685	59.50
	1.32	-3.9643	-1.1560	70.84
HSSA	1.08	-1.8633	-1.5899	14.67
	1.20	-2.4168	-2.1085	12.76
	1.32	-3.0968	-2.7093	12.51

VII. Conclusion And Recommendation

MTCMOS design has significant impact between sensing delay and bit-lines difference. Smaller *ΔBL* as well as smaller delay can be obtained by using MTCMOS design, thus increase performance of particular sense amplifier.

Further study may deeply focus on minimizing the leakage current since low-Vth model experience more leakage current, thus increase unwanted power dissipation. By applying high-Vth seems to be proper method to overcome leakage current [5] but may increase delay and power. Some sense amplifier such as CTSA and HSSA require larger bit-lines voltage difference to operate properly, thus increase noise and the sense amplifier become insensitive.

The varied VDD simulations shows which sense amplifier consumed more power than another. The data shows HSSA consumed largest power consumption as compare to other. So HSSA may not tolerate for low power design SRAM if low power is the top priority. CTSA may perform better for low power and low speed. CSA may perform better for high speed with low power application.

Further study may focus on how to control *WL* pulsewidth to be just sufficient enough or at very short time [7], to create *ΔBL* rather than by letting it turn ON for the whole evaluation phase.

Reference [7] and Reference [8] emphasised to use replica bit-lines for sense amplifier enable for better sensing enable. Replica bit-lines requires additional circuitry for *SAEN* pulse before being fed into sense amplfier.

VIII. References

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