Implementation of VLSI Architecture in Linear Prediction Algorithm

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***Abstract*—This project presents the implementation of VLSI architecture in linear prediction algorithm. The system is designed to monitor the condition base of engine oil and predict the lifetime of the sample of engine oil. The design used for this system is Verilog language. The design is implemented in FPGA board to show the value of slope. This project covered the designing of the Prediction Algorithm where it monitors the degradation of engine oil for real time. The lifetime of engine oil can be predicted based on the value of slope. Synthesis and simulation is done using Xilinx ISE software to obtain the RTL schematic as well as the waveform of the module.**

***Index Terms*— Linear prediction (LP) algorithm, FPGA, Xilinx ISE**

I. INTRODUCTION

Nowadays, lubricant has become a demand. It is true that all engines need the lubricant to operate. To reduce the frequency of changing the lubricant, a system is needed to monitor the basic activity of the lubricant. Many factors contribute to the motor oil's demise. Many cars are now able to utilize an algorithm in the ECU to determine the required oil change interval. It is based on a number of factors such as duration of use, ambient temperature, speed and acceleration. The problem comes when the warning limit is detected. The warning limit is reached when the slope is degreased gradually. To check the warning limit, the slope from origin needs to be checked. That is why the Prediction Algorithm has been designed to overcome this problem.

An algorithm is a step by step calculation used for calculating mathematical functions, data processing, and automated reasoning. It is the effective to calculate mathematical functions. There are many types of algorithm such as linear and polynomial. The linear prediction (LP) algorithm is a famous method applied to space-domain estimation which is MEM algorithm[1]. This algorithm is used to analyze one or two complex sinusoidal signals in additive white noise. LP algorithm is also used to describe high performance packet loss concealment algorithm which is used for pulse code modulation. It uses periodic replication to generate an approximation for the excitation signal of missing speech[2]. LP algorithm has also been used for the detection of land mine.

The algorithm used for this project is linear prediction (LP) algorithm. LP algorithm is the method used in monitoring the degradation of engine oil. The monitoring system can be predicted by using least square method where the best straight line can be determined from the data of the sample. From the straight line, the slope can be defined. The warning limit depends on the value of slope.

The Prediction Algorithm module consists of modules of adder, substractor, multiplexer, and demultiplexer. There are three outputs of the Prediction module which are Slope, SSxx, and SSxy. The Slope is the only output that is connected to the LCD driver. The LCD driver is designed for the implementation of the Verilog codes on the Spartan 3E board

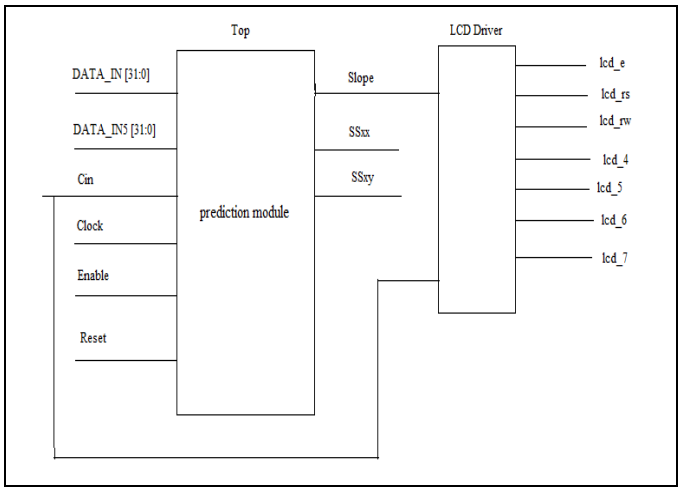

Fig 1. Block Diagram

II. METHODOLOGY

A. Equations

The equation for least square method:

$$y = \beta_0 + \beta_1 x \quad (1)$$

$$\text{Slope } (\beta_1) = \frac{SS_{xy}}{SS_{xx}} = m \quad (2)$$

Where;

$$SS_{xy} = \sum_{i=1}^{n} x_i y_i - \frac{(\sum_{i=1}^{n} x_i)(\sum_{i=1}^{n} y_i}{n} \quad (3)$$

$$SS_{xx} = \sum_{i=1}^{n} (x_i - \bar{x})^2 = \sum_{i=1}^{n} x_i^2 - \frac{(\sum_{i=1}^{n} x_i)^2}{n} \quad (4)$$

x_i = time
y_i = variable of % transmittance
m = the slope of the regression line y axis
n = number of values or elements

The least square method represents the relationship of the independent variables x and dependent variable y. The technique used to determine the best straight line of the data is linear regression.
Linear regression makes four important assumptions:

1. y values are independent.
2. For each x_i, there are an infinite number of possible values of y, which are normally distributed.
3. The distribution of y given a value of x has equal standard deviation for all x and is centered about the linear regression line.

The means of the distribution of y at each x value can be connected by a straight line $y = mx + c$.

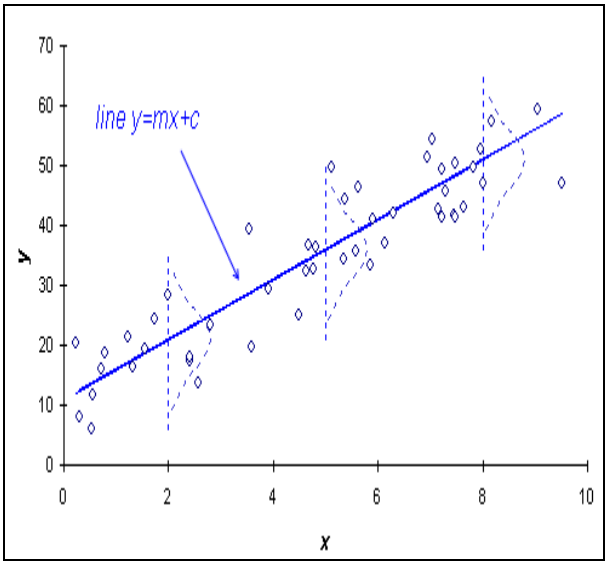

Fig 2. Linear Regression

Fig 2. shows that the linear regression. The best straight line has been taken between the data plotted.

A. Software development

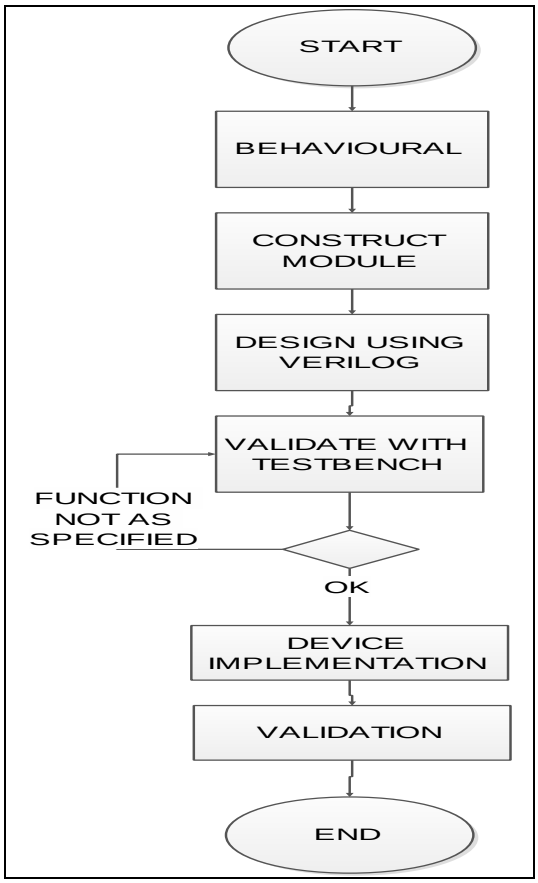

Fig 3. Design Flow

Fig3 . shows the design flow of the project. The design begins with the behavioural of the module. The input and output of the module is specified. Next, the block diagram of the module is designed. The block diagram shows the overview of the module. After that the module is designed using Verilog. The Verilog is designed using the Xilinx software. Once coding is done, the testbench is conducted. The simulation of the module is observed to verify the functionality of the module. If the functionality is correct, the design is implemented on FPGA. The device runs the coding and finally the behavior of the device is observed.

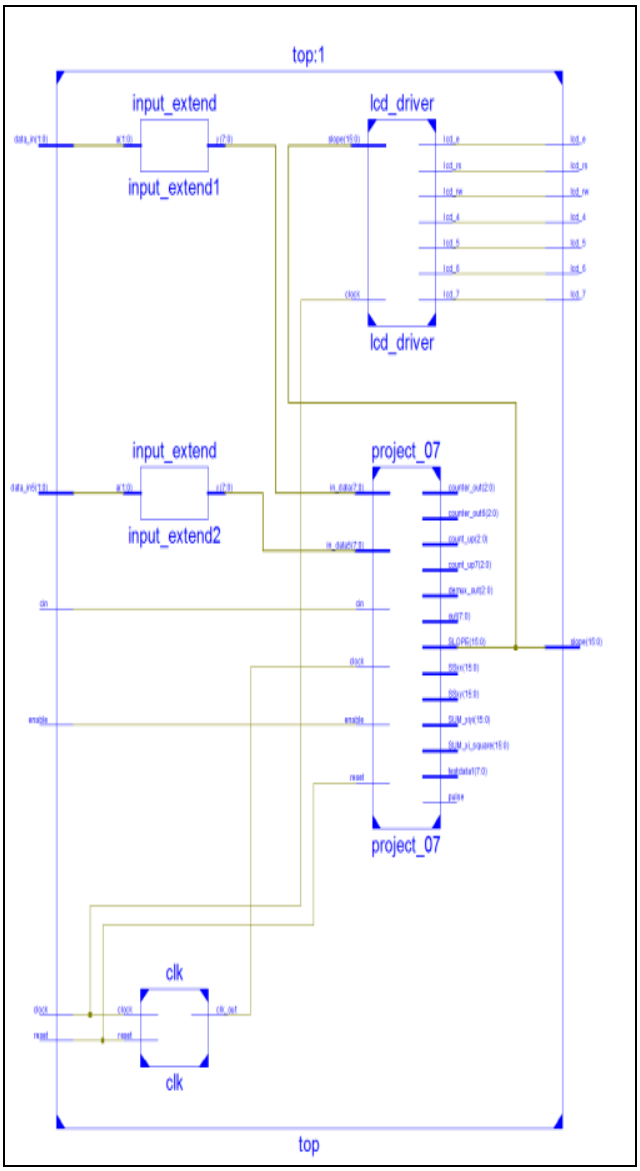

Fig 4. RTL Schematic

Fig 3 shows the RTL schematic of the project. The schematic has been taken form Xilinx ISE after the programming has been done. There are two modules of input extend. The modules are designed because of the limitation on the Spartan 3E FPGA board. The board has only four switches where two switches are for 2-bits. The input data of the project's module is 16-bits. Thus, the combination of the switches could be done until 16-bits. The LCD driver's function is to display the value of slope.

B. Hardware development

Spartan 3E FPGA board has been used to interface with the Xilinx ISE. LCD display is used to display the value of slope. The board is configured using hardware description language (HDL). FPGA contains programmable logic components which is a hierarchy of reconfigurable interconnects that allow the components to be wired together.

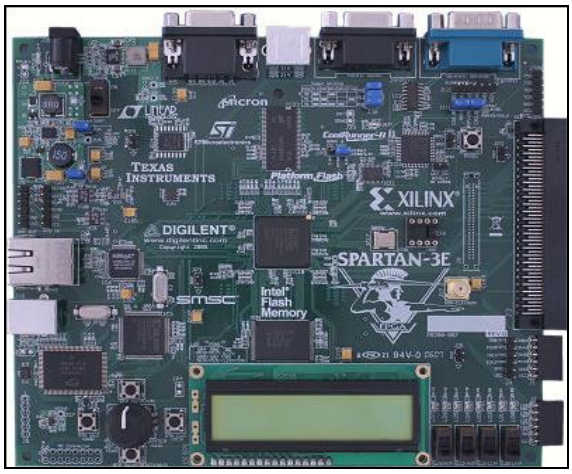

Fig 5. Spartan 3E Board

III. RESULT AND DISCUSSION

C. Simulation

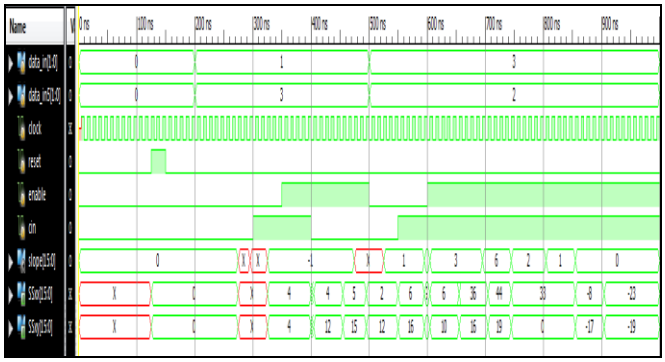

Fig 6. Simulation

Fig 6 shows that the simulation of the project. The value of slope is calculated by SS_{xy} divided by SS_{xx}. Due to the formula of the slope, the slope value shown above is correct. But, the slope has been delayed about 200ns. The delay is caused by the core generator constructed in the divider module. The Spartan 3E board cannot read the divide function in the programming. So, the core generator has been constructed to overcome this problem. The value of the slope is shown in Table 1.

Time(ns)	Data_in	Data_in5	SS_{xy}	SS_{xx}	slope
0	0	0	X	X	X
130	0	0	0	0	-1
280	1	3	X	X	X
330	1	3	4	4	1
400	1	3	12	4	3
460	1	3	15	5	3
500	3	2	12	2	6
550	3	2	16	6	2
600	3	2	10	6	1
650	3	2	16	36	0

Table 1. Simulation Output Data

Table 1 shows the simulation output data of the testbench. The formula of the slope is proven. In the simulation, the decimal value is not displayed. The negative value happens when SS_{xy} *is 0.*

B. Implementation on Spartan 3E board

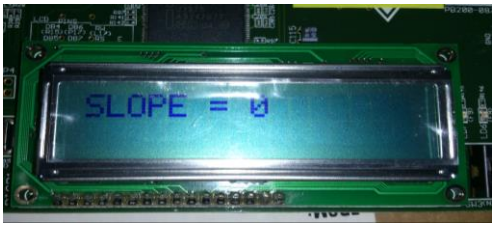

Fig 7. LCD display when slope = 0

Fig 7 shows that the value of slope is 0 which is an error. It happens because the value at the *y* axis is 0. That means the line is parallel with *y* axis.

Enable	C_{IN}	DATA_IN (*x*)	DATA_IN5 (*y*)	Slope
1	1	0	1	-3
1	1	1	1	-7
1	1	1	2	1
1	1	1	3	2
1	1	2	2	1
1	1	2	3	1
1	1	3	3	1

Table 2. FPGA Result

Table 2 shows that the FPGA result after implemented on the Spartan 3E board. The values of the slope displayed on the LCD screen depend on the value of DATA_IN (*x)* and DATA_IN5 (*y)*. The value of *x* and *y* was setup from the switch of Spartan 3E board.

There are several limitations on the board during implementation process. The limitation was the limited switch on the board and the LCD cannot display a value of more than 10 and less than -10.

IV. CONCLUSION AND FUTURE RECOMMENDATION

In this paper, it shows the implementation of LP algorithm on FPGA board. The process starts from designing a Verilog file using Xilinx ISE until the implementation of the design on the Spartan 3E board. The testbench simulation shows that the theory is proven. However, there are some problems that have occurred during the implementation of the design on the Spartan 3E board because of the limitation of switches on the board. For the future recommendation, I suggest that the development of this project should use the FPGA board that can support 32-bits of Verilog programming. With this project, the lifetime of engine oil can be predicted.

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