Design of 8T SRAM and Sense Amplifier Using 0.18 μm CMOS Technology

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Abstract- **In this work, 8T SRAM and sense amplifier (SA) for 0.180 μm with 1.95 V supply at 0.5 MHz CMOS technology were designed. SRAM operation is to retain data content as long as an electric power is supplied to the memory devices, and does not process for rewrite or refresh data. Also, the SRAM cell is preferred because of its low power operation. The performance of SRAM is measured by its static noise margin (SNM) - a measure of the cell's stability to retain its data state. SA is used to translate small differential voltage to a full logic signal that can be further used for digital logic. The choice and design of SA in this work defined the robustness of bit line sensing where the design will impact the read speed and power. Thus, modified current sense amplifier (MCSA) was chosen for the 8T SRAM of this work. The finding reveals that performance of 8T SRAM with MCSA results the operating speed of 104.947 ps and the power consumption was reduced from 43.792μW to 11.3362μW**

Keywords-8T SRAM, power consumption, static noise margin, sense amplifier.

I. INTRODUCTION

SRAM is defined as Static Random Access Memories. Its function to retain data content as long as electric power is supplied to the memory devices, and do not need any rewrite or refresh operation. SRAM also is a type of volatile semiconductor memory to store binary logic '1' and '0' bits, and uses bi-stable latching circuitry made of transistors or MOSFETS to store each bit [1]. The issues of designing SRAM generally cover area, lower power and noise margin [2]. The issue of area in 8T SRAM is due to an addition of PMOS in the feedback of the latch in write operation in the 7T SRAM cell's write capability. The low power issue in the 8T SRAM cell occurs when there is a reduction of the supply voltage. Thus the power dissipation is reduced. Also power dissipation in the SRAM cell is contributed from the operating temperature and frequencies [2]. Some literatures have shown that, 10T modified SRAM cell at the 90 nm and 45 nm technology, and 10T SRAM cell at the 32 nm technology has better performance for the temperature and frequency [2]. The static noise margin (SNM) issue on the 8T SRAM cell occur when the V_{DD} is lower, the gate current will be reduced and much more rapidly than the sub-threshold current and consequently degrade the SNM. This degradation of SNM can further limit the voltage scaling [2].

In contrast, SA is used to detect stored data from a read-selected memory cell [2]. The SA also is used to translate the small differential voltage to a full logic signal for further used by digital logic [3]. In addition, SA is different in the electrical balanced symmetric circuits, because of the process variation where all the devices in the circuit do not have the same characteristic. The SA requires more strength in the SRAMs by its redundancies where their sizes are not scaled [3]. This is because of the tradeoff between their statistical offset and their physical size. The sensing and amplifying of the data signal will transmit passes through memory cell to bits line which is mostly an important function to the sense amplifiers. Furthermore, the SA also must in high performance for low power SRAMs [3]. Therefore, the purposes of this work were aimed to design 8T SRAM and SA using 0.18 μm CMOS technology. The design was made for 1 bit, 4bit and 8bit 8T SRAM with SA technique to improve SRAM performance.

In this work, the design of SRAM comprises of 8 transistors with SA for CACHE specification of 2 KB N-way set associative. The CACHE holds the write-back data and writes it into main memory when that data line in CACHE is to be replaced. In this project, the design of 8T SRAM will consider the process variation for low power application to achieve low power consumption and speed using 0.18 μm CMOS process and achieves functionality at 0.5 MHz and voltage supply V_{DD} of 1.95 V. The result shows that 8T SRAM with MCSA achieved the operating speed of 1.04947 ps and the power consumption was reduced from 43.792μW to 11.3362μW.

II. DESIGN IMPLEMENTATION

A. 8T SRAM Cell Design

Figs. 1 and 2 depict the overall block diagram of 8T SRAM with two different types of SA respectively. Both topologies were evaluated and Fig. 1 was used to investigate the performance of 8T SRAM with MCSA. This is because MCSA enhances the speed of the sense amplifier further due to the fact that there is a flow of bias current before the SA is actually enabled [5].

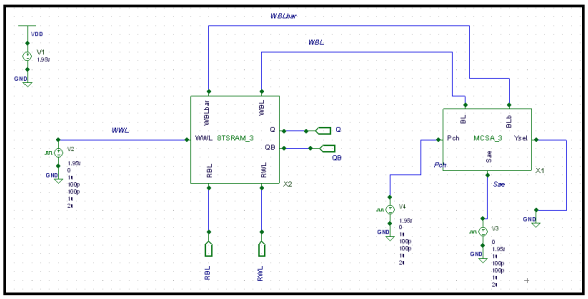

Fig 1: The Schematic of 8T SRAM with MCSA

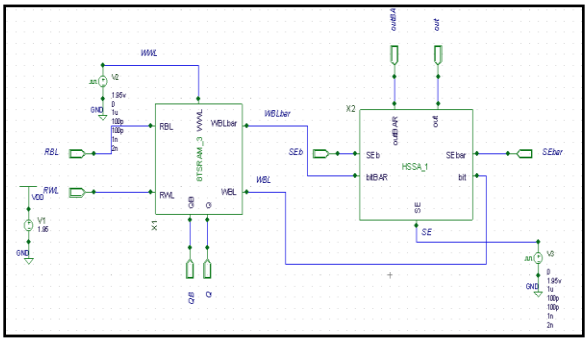

Fig 2: The Schematic of 8T SRAM with HSSA

Fig. 3 shows the schematic of 8T SRAM cell used in this work. M1 and M2 is PMOS transistor and M3-M8 is NMOS transistor. As shown in the schematic, transistors M1-M4 form a cross-couple structure to store data. Meanwhile, transistors M5-M8 are access to the internal nodes Q and Qbar (QB) of the cell. The transistors N5 –N6 connect the cell internal nodes Q and QB of the cell. Also, N5-N6 connect to the write word line (WWL) and writes bit line (WBL) while transistor M8 connect to Read bitline (RBL) and read word line (RWL). Furthermore, two PMOS transistor labeled M1-M2 are sources that connects to the V_{DD} of 1.95 V.

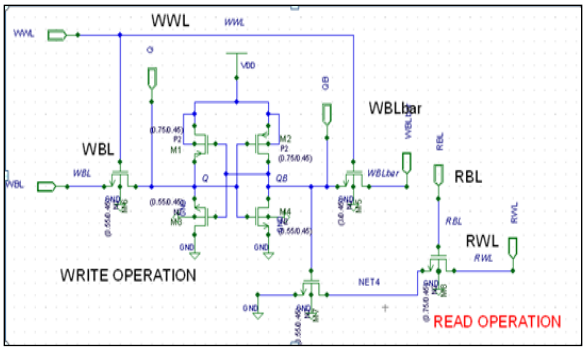

Fig 3: The schematic of 8T SRAM

The operation 8T SRAM consisted of read (R) and writes (W) cycles. If W is in logic '1' operation, the world bit-line bar (WBLbar) will pull down to the threshold voltage $-V_{tn}$ of M5. Thus node QB will start discharging and turn ON M1. When the M1 is turned ON, the node Q is at logic '1' and hence logic '1' is written into the cell. If W is in logic '0' operation, the WBL is pulled down to the logic'0'. The signal WWL will rise from logic '0' to logic'1' promptly and turn OFF M5. In addition, the node Q starts discharging and turn ON M2 which causing cell to flip and logic '0' is written into the cell.

For R operation, two WBL and WBLbar are held at logic '1' by the pre-charged circuitry. If R is in logic '1' operation, WBL will remains at logic'1' because node Q is stored at logic '1'. Also, the single ended SA output remains at logic '1'. If R is in logic '0' operation, the WBL will start discharging through M6 and M3 thus the SA will produce logic '0' when WBL falls below a certain threshold voltage.

B. Sense Amplifier

Sense amplifier (SA) is the most critical circuits in the CMOS memory. The performance of SA will strongly affects both memory access time and overall memory power dissipation. In addition, SA is used to translate small differential voltage to a full logic signal that can be further used by digital logic [3]. The need for increased memory capacity, higher speed and lower power has defined a new operating environment for future SA. Thus two types of SA were proposed - MCSA and HSSA as shown in Figs. 4 and 5 respectively. However, the schematic of Fig. 4 is used for the 8T SRAM because the speed and current cell are smaller compare with HSSA.

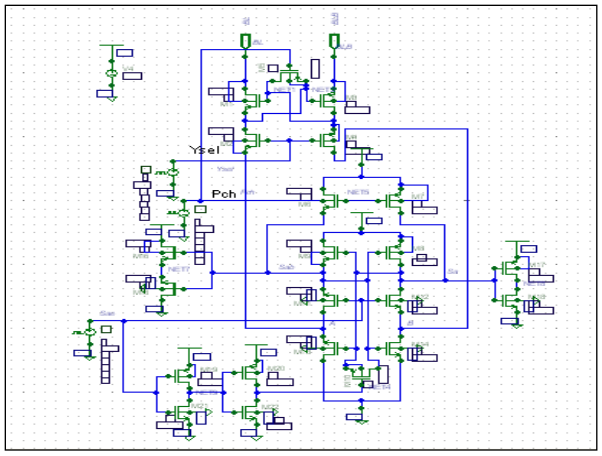

Fig 4: The Schematic of Modified Current Sense Amplifier

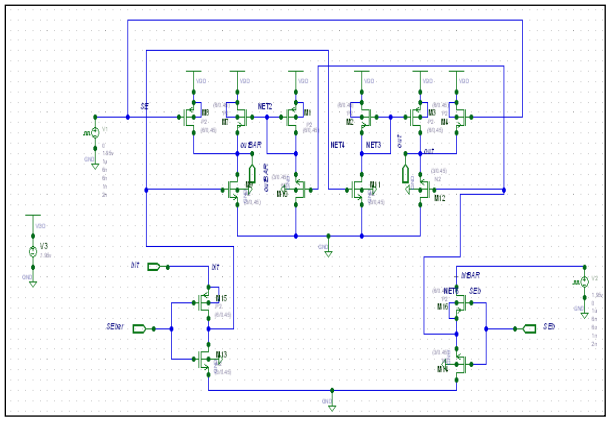

Fig 5: The Schematic of High Speed Sense Amplifier

III. RESULT ANALYSIS AND DISCUSSION

A. 8T SRAM

Figs. 6 and 7 exhibits the simulation result of 8T SRAM using 0.18 µm technology for Read and Write operation state respectively.

Fig. 6 is the output of 8T SRAM at read operation. The read operation consist of two transistor NMOS (M7 and M8) to improve the read stability [4]. The cell nodes are decoupled from read bit-lines (RBL) via read devices M7 and M8. When read wordline (RWL) is enabled, the read bit-lines (RBL) are conditionally discharged based on the cell data [4]. This is because of cell nodes are decoupled from the RBL.

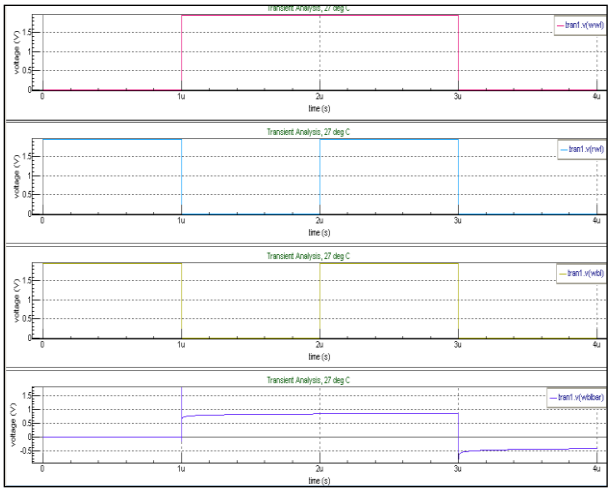

Fig 6: The Output 8T SRAM at Read Operation

Fig. 7 depicts the 8T SRAM at Write operation. As mentioned previously, Write operation is executed by enabling the write wordline (WWL) after loading the data onto the write bit-lines (WBL,WBLbar). The current ratio between the write access transistors NMOS (M6 and M5) and the pull-up transistors PMOS (M1 and M2) determined the cell write margin.

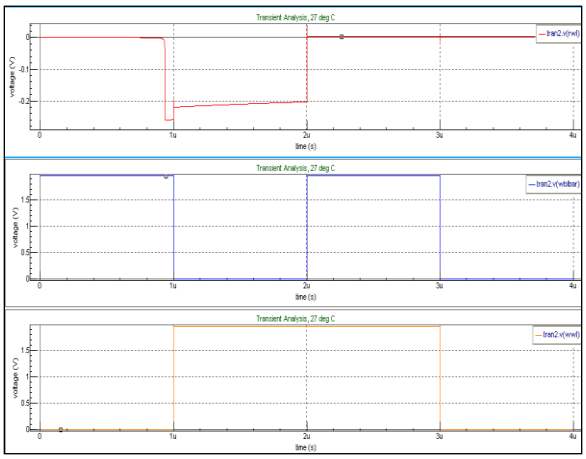

Fig 7: The Output 8T SRAM at Write Operation

Table 1 showed the comparison of the performance between Read and Write operations. Here, the speed at Read port is 753.25 ps are smaller compared to write port is 1.002 ns. This is because each Read port is connected to the complementary RBL where it improves Read speed and reduces the bit-lines discharge power with small voltage differential amplification [5]. While the power dissipation is reduces from Write to Read operation specifically from 11.278 nW to 0.295 nW.

Table 1: The Comparison or Read/ Write Operation 8T SRAM

Criteria	Access Time (Speed)	Power Dissipation (Watts)	Current
Read Operation	753.25p	2.9469e-010	7.3782e-0 fA
Write Operation	1.002n	1.1278e-008	1.2566 pA

B. *Signal Noise Margin*

Another parameter for 8T SRAM is signal noise margin (SNM). The SNM is the maximum amount of noise voltage that can be introduced at the output of the two inverters, such that the cell retains its data [6]. SNM quantifies the amount of noise voltage required at the internal nodes of a bit-cell to flip the cell's contents. The SNM is also defined as the length of the side of the largest square that can be embedded inside the lobes of the butterfly curve.

Fig. 8 exhibits the SNM of 8T SRAM of this work. There are two operating modes - Read and Write. Each mode can define its own operating margin. Here, the SNM of this work is decrease 0.12 time compared with Ref. [7] value is 1.22. Where the calculation of SNM is

$$V_{OH}\text{-}V_{OL}= 0.12 \text{ V}.$$

This design is better from [7] because the frequency used for this work was 0.5 MHz and Ref. [7] used frequency of 200 MHz. Generally, the decrease of SNM is also due to high V_{DD} [10] [14] where this work employed V_{DD} of 1.95 V.

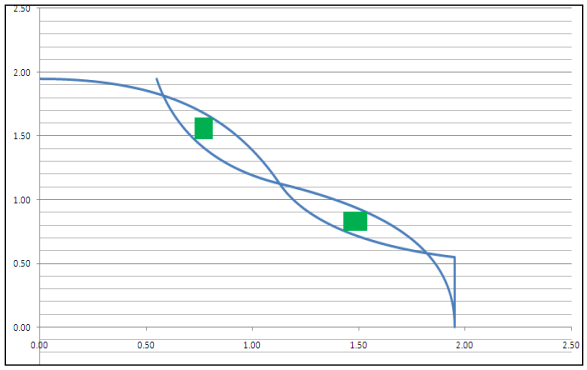

Fig 8: The 8T SRAM of SNM

As shown in Table 2, the result depicts the comparison of SNM between this work and the [7].

Table 2: Comparison this work and reference

	V_{DD}	Frequency (MHz)	SNM
This work	1.95V	0.5	0.12
[7]	1.2V	200	1.22

C. *AREA OF 8T SRAM*

The analysis of area is performed for the layout of 8T SRAM using 0.18 µm CMOS technology. Its minimum size is scaled down, which enables higher density and lower chip cost like large capacity SRAMs for storing data, smaller area SRAMs are required in terms of chip cost and yield.

Fig. 9 depicts the layout of 8T SRAM using Expert tools. From the layout the area is 4.370 µm × 7.4950 µm. The area of 8T SRAM is higher compared to conventional 6T and 7T SRAM.

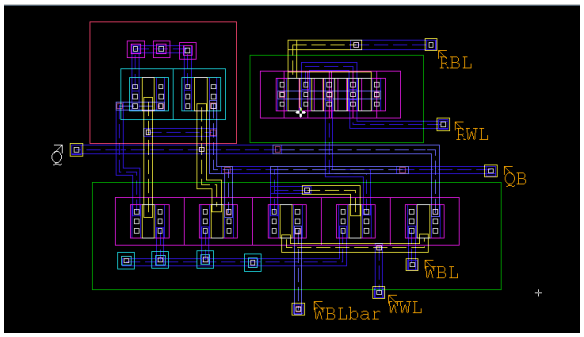

Fig 9: The Layout of 8T SRAM

D. *8T SRAM with Sense Amplifier*

As mentioned previously, the design of 8T SRAM with MCSA was investigated. In this work, the speed, the power dissipation and the power consumption were compared for 1 bit, 4 bit and 8 bit data between 8T SRAM and 8T SRAM with MCSA.

As shown in Fig. 10, the finding reveals the speed of 8 bit 8T SRAM with MCSA is reduced. The speed for 8 bit SRAM with MCSA is of 29.083ps. This is because SA is used to translate small differential voltage to a full logic signal that can be further used by digital logic. Furthermore, the MCSA enhances the speed of the SA further due to the fact that there is a flow of bias current before the SA is actually enabled [8]. As mentioned previously, this work used this topology for the investigation of speed and

power because the design revealed better performance compared 8T with HSSA.

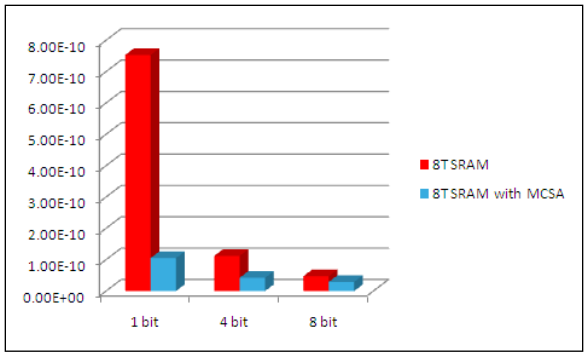

Fig. 10: Access time (Speed) of 8T SRAM with MCSA

Fig. 11 results revealed that power dissipation increases as the bit increases. This is because as the density of SRAM cell on chip increases, there are some concern towards excessive power dissipation continues to rise [8][9] as shown in this work.

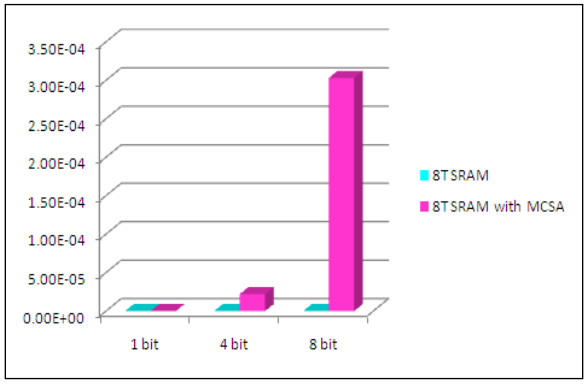

Fig 11: Power dissipation of 8T SRAM with MCSA

Fig. 12 showed that power consumption of 8T SRAM with MCSA for 1 bit, 4 bit and 8 bit. The analysis was obtained from the measure of power consumption during Write operation from the BL and WL switching power [10] [11]. The power consumption was achieved to improve as the bit increases. The result shows the power consumption was reduced from 43.792 µW to 11.3362 µW. Thus, this finding shows that the need for increased memory capacity, higher speed and lower power consumption has depended to sense amplifier used.

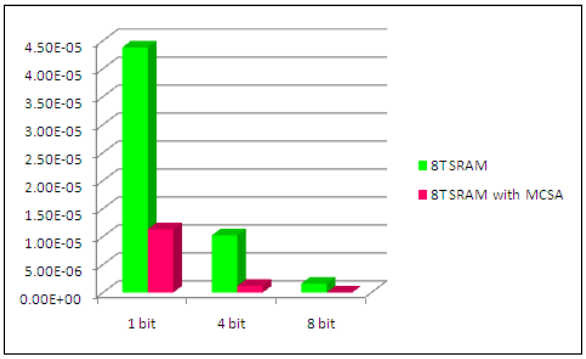

Fig 12: Power consumption of 8T SRAM with MCSA

As shown in Figs. 11 and 12, the power consumption was larger compared to the power dissipation. This is because the current in SA was made enable with the depicts the finding of power dissipation for 1 bit, 4 bit and 8 bit 8T SRAM with MCSA. The intention that current sensing does not depend on differential discharging of large bit-lines capacitance [12]. However, the energy was saved with reduced bit-lines swing and compensated by the power dissipation of SA[13]. The sense amplifier is used to amplify the small bit-lines signal and eventually drive it to the external word.

IV. CONCLUSION

In this paper, 8T SRAM with MCSA using 0.18µm CMOS technology has shown improvement to the capacity, high speed, and low power in the 8T SRAMs cell. The analysis of the work was compared between 8T SRAM and 8T SRAM with MCSA.

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