Investigation of Shallow Trench Isolation and Silicide Effect on 90nm CMOS Devices

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Abstract – **To investigate the stress effect on device performance, a 90nm Complementary Metal Oxide Semiconductor (CMOS) was designed and simulated. Strained technology is used to enhance the performance of the CMOS that involves physically stretching or compressing the silicon crystal lattice, which in turn increasing carrier mobility without having to make them smaller. Shallow-trench isolation (STI) and silicidation process is the way of strained technology process applied in this investigation. This paper discussed on the effect of strain technology on 90nm CMOS device performance focusing on threshold voltage and drain current parameter. Athena and Atlas simulators were used to simulate the process and to characterize the electrical properties respectively. It can be concluded that CMOS with STI and Silicide have better performance than the conventional CMOS. It shows that drain current with STI have been improved by 10% in PMOS and 90.7% in NMOS. While by using Silicide it shows 5.4% in PMOS and 1.82% in NMOS improvement.**

Keyword: Compressive stress, Tensile stress, Shallow trench Isolation (STI), Silicide.

I. INTRODUCTION

The used of CMOS are increasing tremendously due to its application in many electronic devices. Over the past 3 decades, the speed and functionality of electronic devices is increasing successfully. The microelectric industry has been looking another method to improve the CMOS device performance. The transistor performance can be improved in three ways which are increasing the CMOS gate capacitance, improving the carrier mobility or decreasing the channel length [1]. Smaller transistor will decrease the power consumption. Furthermore, the cost of making the transistor smaller and faster is becoming very expensive and the current is tend to leak even there is no voltage applied to the transistor if the transistor become small and thin. These situations cause the microelectric industry face serious cost and technical challenges in order to maintain its power consumption.

One of the best alternative to get the faster devices perform at power level is by improved the carrier mobility of the transistor. In order to improve the carrier mobility the strained technique is being used [2]. The basic functional relationship for CMOS due to drive current is given in the equation below:

$$Id = \beta/2\ (V_{gs} - V_t)^2 \qquad (1)$$

where,

$$\beta = \mu * C_{oxide} * (W/L) \qquad (2)$$

An important and promising feature of strained silicon for future technology is that it increases device performance without decreasing the channel length or increasing the off-state leakage current There are 4 methods in strained technique which are Shallow Trench Isolation (STI), SiGe (Silicon Germanium), Silicidation process and silicon nitride (Si_3N_4) capping layer [3]. In this paper, two techniques had been covered to enhance the performance of 90nm CMOS devices which are STI and Silicide process.

II. SCOPE OF WORK

A. Shallow Trench Isolation

Figure 1 show the illustration of STI. STI etch process is used to create shallow trench in Si substrate which are subsequently with dielectric material to form barrier between device element. While allowing a higher packing density, STI structures are becoming major contributors to the mechanical stresses present in the silicon substrate. To create an STI structure a trench is etched into the silicon using reactive ion etching (RIE). Next the trench walls are lined with a thin layer of SiO_2 by thermal oxidation. The trench is then filled with 40 chemical vapor deposition (CVD) SiO_2, another CVD dielectric or CVD polysilicon. Finally, the structure is chemical mechanical polished (CMP), and a planar STI structure is created [4].

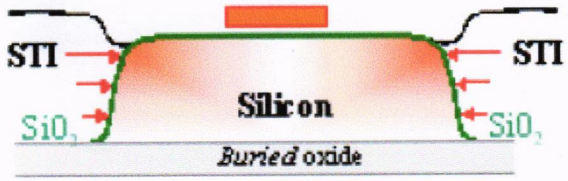


Figure 1: Illustration of STI

B. Silicide

Metal silicide like nickel silicide (NiSi2) used to obtain compressive stress in the PMOS channel [5]. Silicides have a higher thermal coefficient of expansion then Si, and patterning them on the top of the PMOS transistors structure leading to higher hole mobility. The advantage of using silicide is low silicon consumption, smaller mechanical stress, low temperature silicidation process and good contact to other material [6]. Figure 2 show silicidation process.

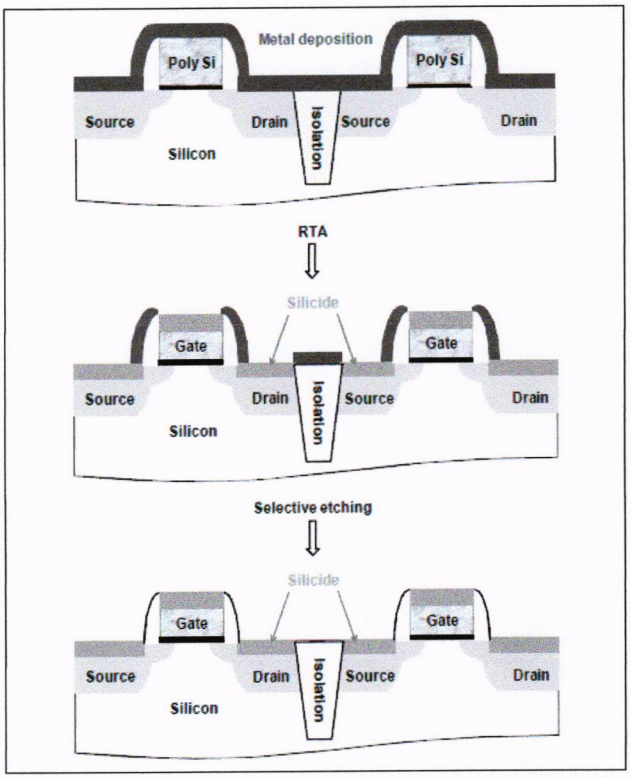


Figure 2: Illustration of SILICIDE process.

III. METHODOLOGY

The design process and device modeling for this paper was done by using TCAD SILVACO software. Athena, Atlas, Tonyplot consist of the Silvaco Suite of applications. Each of them has their different uses and controlling applications. Athena is used for creating the fabrication design process such as layer deposition, lithography, etching, implantation, diffusion and oxidation. Atlas is used for modelling fabricated designs and extracting device parameters. Tonyplot is used for creating visual representations of the simulations. Together, they accurately allow a user to simulate and test devices of a production wafer fabrication process [7]. Silvaco will expose the device what should actually behave, and identify the electrical characteristic of the CMOS.

This project will involve with design, modeling and simulation of NMOS and PMOS transistors for a 90nm device using strained technology. Figure 3 shows the steps for the CMOS design using Silvaco.

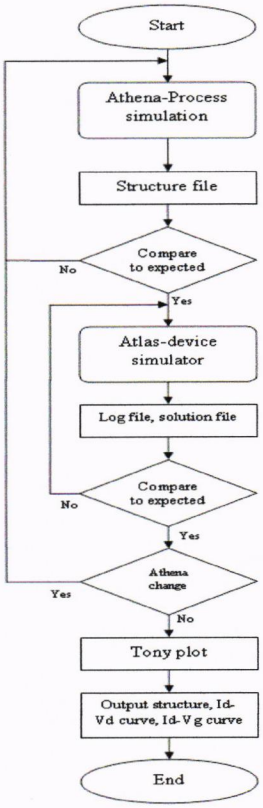


Figure 3: CMOS Design flow chart.

IV. RESULT AND DISCUSSION

A. Shallow Trench Isolation.

Figure 4 shows the completed 90nm NMOS transistor with STI technology using Athena. At this point the physical construction of the device is complete. Atlas will be used in order to obtain device characteristics, such as threshold voltage and drain current. Figure 5 show the electrical characteristic curve for NMOS with STI. In order to establish what the turn-on voltage of the transistor is, the I_d-V_g curve was plotted. Figure 5(a) is show the I_d-V_g curve where the drain voltage is set to 0.1V. Figure 5(b) shows the I_d-V_d curves and the applied gate voltages of 1.1V, 2.2V, and 3.3V were applied to the device.

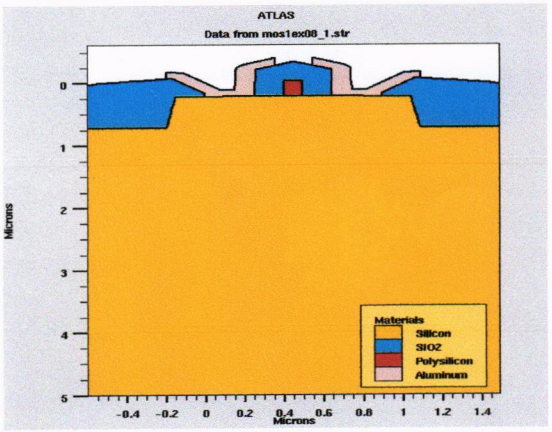
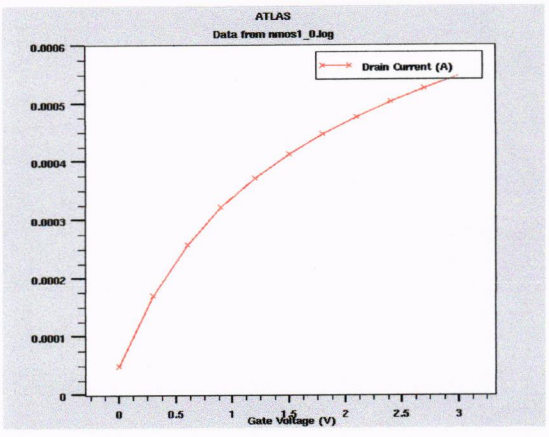
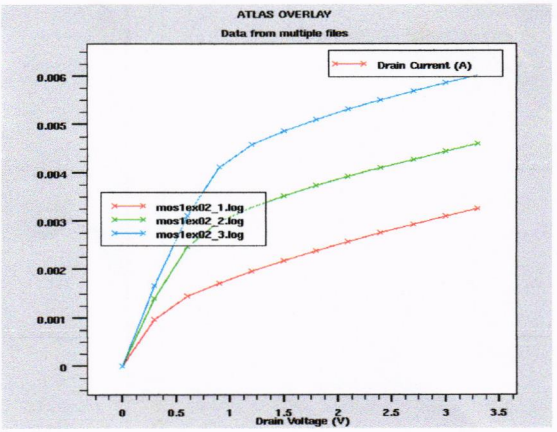


Figure 4: Design of 90nm NMOS with STI.



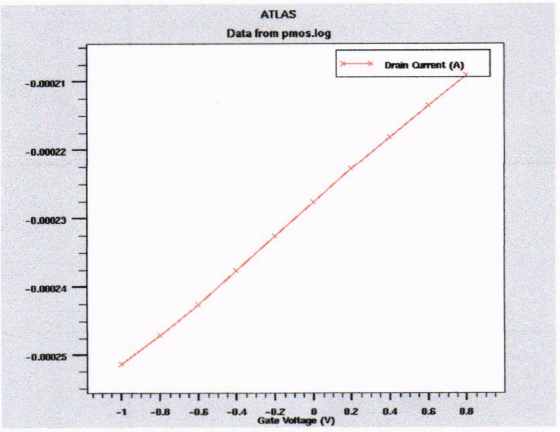
(a) : I_d-V_g curve



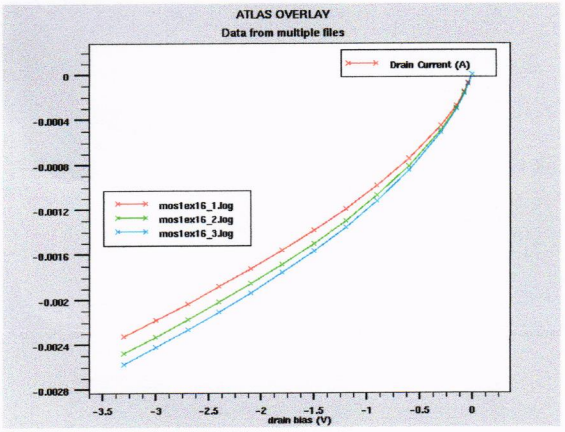
(b) : I_d-V_d curve

Figure 5: Electrical characteristic curve for NMOS with STI.

Figure 6 show the electrical characteristic curve for PMOS with STI. Figure 6(a) is show the I_d-V_g curve where the drain voltage is set to -0.1V. Figure 5(b) shows the I_d-V_d curves where the transistor at applied gate voltages of -1.1V, -2.2V, and -3.3V were applied to the PMOS.



(a) : I_d-V_g curve



(b) : I_d-V_d curve

Figure 6: Electrical characteristic curve for PMOS with STI.

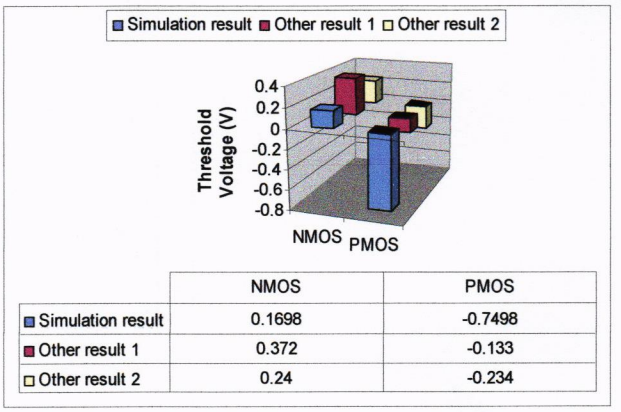
Table 1 shows the electrical characteristic of CMOS with STI and without STI. From equation 1 and 2, it show when drain current increase which in turn improve the mobility, it will increase the device speed. Result shows that CMOS with STI technology having higher I_d and V_t. The higher value of Id and Vt will give the best result for NMOS but for PMOS the higher value of negative result value will show the best result.

Drain current for both NMOS and PMOS were improving with NMOS increase 90.7% while PMOS improve 10%. For threshold voltage, PMOS seem to have no difference change with STI or without STI and for NMOS it improves 26.8%.

Table 1: Electrical characteristic of CMOS with STI and without STI

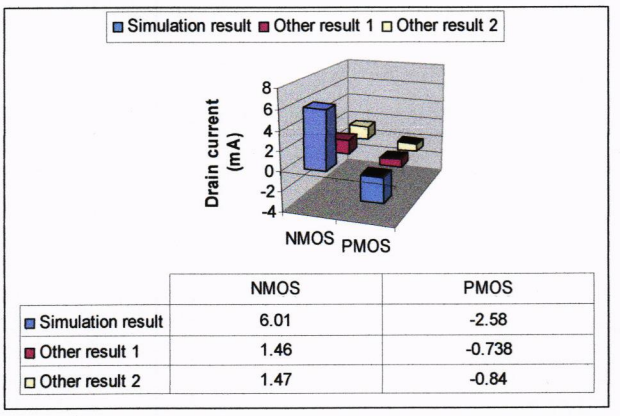
	Vt (V)		Id(mA)	
	NMOS	PMOS	NMOS	PMOS
STI	0.1698	-0.7498	6.01	-2.58
Without STI	0.1242	-0.7497	0.559	-2.32

Figure 7 and 8 shows the comparison of STI with other research due to drain current and threshold voltage. From this result, CMOS with STI from this research has higher drain current and threshold voltage for PMOS. A 140nm CMOS device with STI has been used to compare this result.



	NMOS	PMOS
Simulation result	0.1698	-0.7498
Other result 1	0.372	-0.133
Other result 2	0.24	-0.234

Figure 7: Threshold voltage comparison of STI with other researches.



	NMOS	PMOS
Simulation result	6.01	-2.58
Other result 1	1.46	-0.738
Other result 2	1.47	-0.84

Figure 8: Drain current comparison of STI with other researches.

B. Silicide

Figure 9 shows the completed 90nm NMOS transistor with silicide technology using Athena and Atlas will be used in order to obtain the threshold voltage and drain current. Figure 10 show the electrical characteristic curve for NMOS. Figure 10(a) is show the I_d-V_g curve where the drain voltage is set to 0.1V. Figure 10(b) shows the I_d-V_d curves that were obtained from our device. The curves show for the NMOS transistor at applied gate voltages of 1.1 V, 2.2 V, and 3.3 V were applied to the transistor, and the drain current was graphed as a function of the applied drain voltage.

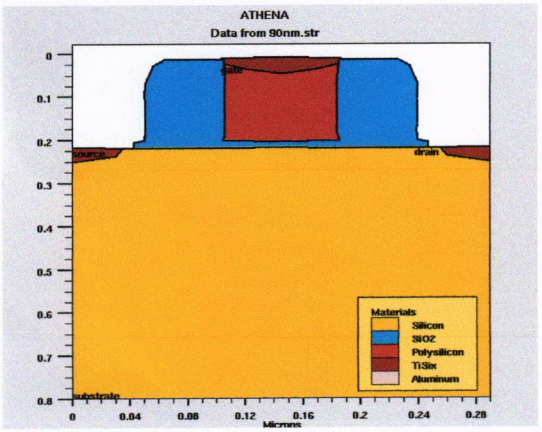
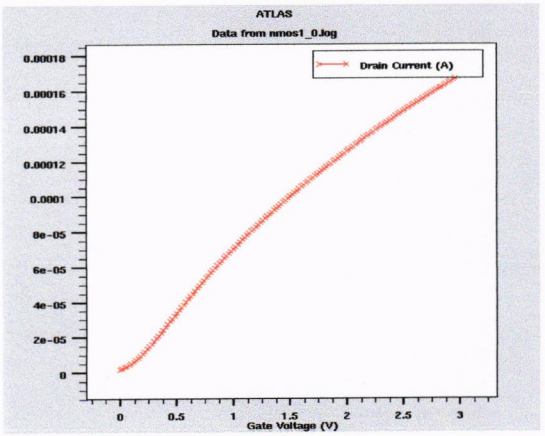
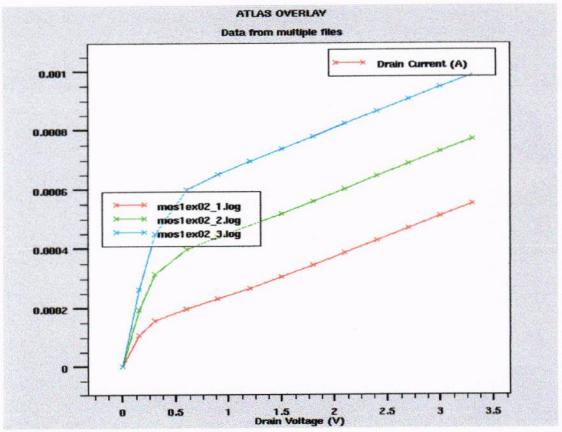


Figure 9: Design of 90nm NMOS with Silicide.



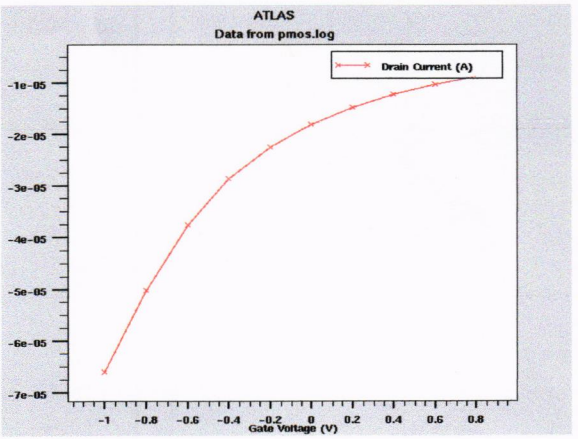
(c) : I_d-V_g curve



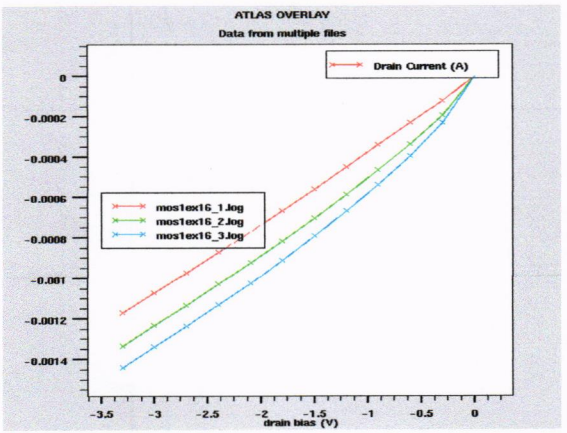
(d) : I_d-V_d curve

Figure 10: Electrical characteristic curve for NMOS with Silicide.

Figure 11 show the electrical characteristic curve for PMOS. Figure 11(a) is show the I_d-V_g curve where the drain voltage is set to -0.1V. Figure 11(b) shows the I_d-V_d curves and the applied gate voltages of -1.1 V, -2.2 V, and -3.3 V were applied to the device.



(c) : I_d-V_g curve



(b) : I_d-V_d curve

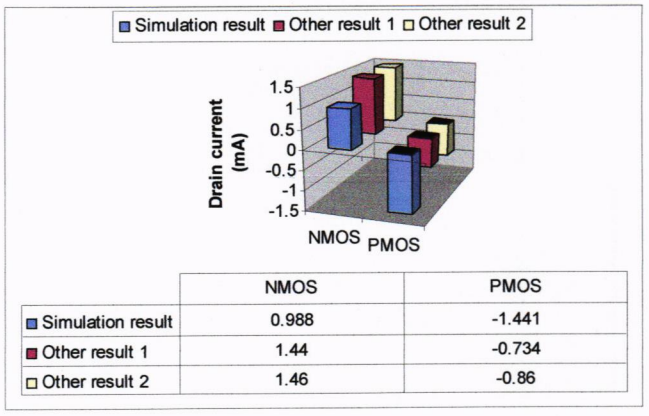
Figure 11: Electrical characteristic curve for PMOS with Silicide.

Table 2 shows the electrical characteristic of CMOS with Silicide and without Silicide. From the table it shows that CMOS with Silicide technology having higher I_d. Drain current for both NMOS and PMOS were improve with NMOS increase 1.82% while PMOS improve 5.4%. NMOS with Silicide technology shows increase 12.5% performance in threshold voltage but having 37% decrease for PMOS. Result shows that strained technology using Silicide have better effect and suitable for used in 90nm CMOS device.

Table 2: Electrical characteristic of CMOS with Silicide and without Silicide.

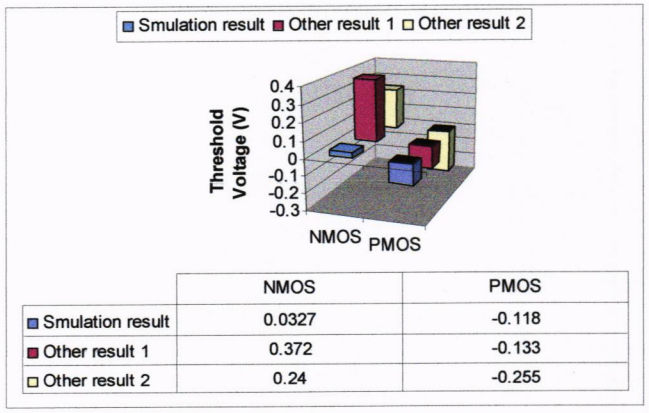
	Vt (V)		Id (mA)	
	NMOS	PMOS	NMOS	PMOS
Silicide	0.0327	-0.118	0.988	-1.441
Without Silicide	0.0286	-0.189	0.970	-1.363

Figure 12 and 13 shows the comparison of Silicide with other research with respect to drain current and threshold voltage. Result show that CMOS with Silicide from this project show higher drain current for PMOS. Thus a selective modification of Silicide strain effect is importance for advanced NMOS.



	NMOS	PMOS
Simulation result	0.988	-1.441
Other result 1	1.44	-0.734
Other result 2	1.46	-0.86

Figure 12: Drain current comparison of Silicide with other researches.



	NMOS	PMOS
Smulation result	0.0327	-0.118
Other result 1	0.372	-0.133
Other result 2	0.24	-0.255

Figure 13: Threshold voltage comparison of Silicide with other researches.

V. Conclusion

From the result, it can seen that the strained technology that involve STI and Silicide have better performance compared to the ordinary CMOS. Further improvement must be done to the device in order to achieve a significant enhancement on CMOS device. Strained technology will give more benefit and very useful in fabricate CMOS device and therefore more research is still needed to improved its implementation to the current technology.

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