# 8T SRAM WITH DIFFERENT TYPE OF SENSE AMPLIFIER

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**ABSTRACT- In this paper, it presents the 8T SRAM by using different type of sense amplifier which is voltage-mode sense amplifier (VMSA) and current-mode sense amplifier (CMSA) stored date. The objectives of this research is to identify which one of these sense amplifier has the most high speed, less delay, and low power dissipation and also has the smallest cell area in layout. Sense amplifiers are one of the most critical circuits in the periphery of CMOS memories. This plays an important role to reduce the overall sensing delay and voltage. Earlier voltage mode sense amplifiers are used to sense the date it sense the voltage difference at bit and bit lines bar but as the memory size increase the bit line and date line capacitances increases. The software that will use for simulation is SILVACO EDA which is Gateway and Expert for layout by using 0.18um technology. The results show that the CMSA has high speed which is has delay 36-46% performed better than VMSA, and low power dissipation is 5-15% compared to VMSA. But, VMSA has the better cell area where it has 31.50% smaller than CMSA and the DRC and LVS for both layouts is shows with no error and equivalent. All the objectives are achieved and it shows that the CMSA has more advantages compare to VMSA and it is suitable for high speed performance and low power circuitry.**

***Index Terms – Voltage mode sense amplifier, Current mode sense amplifier, SRAM, design rules check, layout versus schematic.***

## I. INTRODUCTION

Technology and supply voltage scaling continues to improve the logic circuit delay with each technology generation. However, the speed of the overall circuit is increasingly limited by the signal delay over long interconnects and heavily loaded bit-lines due to increased capacitance and resistance[1].

Static Random Access Memory (SRAM) is a type of semiconductor volatile memory (RAM) which keeps its data until the power is turns OFF. SRAM will store the binary logic bits '1' or '0' [2]. It consists of an array of memory cells along with the row and column circuitry. SRAM has design to fill two needs that are to provide direct interface with CPU at speeds not achievable by DRAMs and to replace DRAMs in systems that require very low power consumption. The stability and area of SRAM need to be concern in designing SRAM cell. SRAM cell must be able to write and read data and keep it as long as the power is applied. The main challenge in designing SRAM cell is to ensure that the circuitry holding the state is weak enough to be overpowered during a write, and still strong enough to be not disturbed during read operation.

SRAM represents a large portion of the chip, and it is expected to increase in the future in both portable devices and high-performance processors. To achieve longer battery life and higher reliability for portable application, low-power SRAM array is a necessity [3].

Sense amplifiers are used to translate small differential voltage to a full logic signal that can be further used by a digital logic. The need for increased memory capacity, higher speed, and lower power consumption has defined a new operating environment for future sense amplifiers. Sense amplifiers are mainly used to read the contents of SRAM and DRAM cells [4] Sense amplifier is one of the important peripheral circuits in memory as it strongly influences the memory access times [3].

This sense amplifier can be operated in voltage, current and charge mode but we operate them in current-mode because they present a low impedance to the inputs and respond to the differential current rather than to the voltage between the inputs, this can reduce interconnect delay in long wires there by providing speed improvement. The current mode sense amplifier reduces the bit line swing during read operation as compared to voltage mode sensing technique. It proves that current sensing technique would be faster than voltage mode due to the low impedance termination of the current mode. It shows that current sensing is relatively insensitive to the bit line capacitance [5]. This gives the motivation to use current mode sensing in the bit lines in SRAM.

In this paper, we explore the design of the 8T SRAM connected with different type of sense amplifier which is voltage mode sense amplifier and current mode sense amplifier by using 0.18um technology process and we compare the various designs based on delay, power dissipation and cell area. The two sense amplifier topologies compared are current mode sense amplifier (CMSA) and voltage mode sense amplifier (VMSA).

## II. CIRCUIT DESCRIPTION

### *A. 8T SRAM*

The 8T SRAM circuit that is used in this simulation is the ultra-low power. It consists two cross coupled inverters which is M1, M2, M3 and M4. There are two extra NMOS

transistors connected to the cross-coupled inverters where each of them pulls down the path of the cross-coupled inverters so that it can achieve the leakage power reduction. In addition, both drain inverters is connected to the NMOS transistors so that it connected to the write-word line (WWL) at their respective gate terminals and the drain is connected to the BitLine (BL) and BitLine_Bar (/BL). The write-word line is used to select the cell while the bit lines are used to perform write and read operations on the cell [8]. Both BitLine and BitLine_Bar are used to improve the speed of write and read operations.

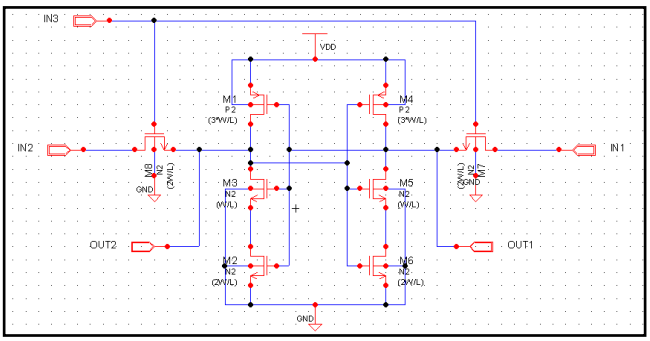


Fig.1: Schematic 8T SRAM

*i. Write and Read operation*

To get the write and read operation, the input BL and BL_Bar and WWL are playing the very important role. Writing a value into the 8T SRAM cell is done by forcing the BL and BL_Bar high while keep the other low. To get the write operation high '1', insert the input WWL '1' and set the BL also '1' and the BL_Bar is '0'. Then the output waveform will get high '1'. Therefore, to get the output Write low '0', BL is made to low and the BL_Bar is made high '1'. Thus the output will get low '0'. Before reading from the SRAM cell both bitlines are pre-charged high and SRAM cell is selected [10]. For read operation, the sense amplifier will take action because sense amplifier are used to sense which line is being pulled down and perform the read operation of the stored data.

Before knowing the operation of 8T SRAM, we must know the operation of 6T SRAM because 8T SRAM circuit is based on the 6T design. There are strict constraints on the size of transistors to receive a suitable beta ratio in a conventional 6T SRAM cell [6]. It becomes harder to ensure a favorable SNM in a read operation when the supply voltage is lowering.

The stability of a 6T SRAM cell under process variation can be verified by examining its butterfly curves obtained by voltage transfer characteristics (VTC) and inverse voltage transfer characteristics (VTC). Under process variation the read static noise margin (SNM) of a standard 6T SRAM cell is shown in Figure 2. One can observe that the SNM window has narrowed down due to process variation and this effect becomes severe at lower $V^{-1}$. The most attracting cell in this direction is referred as read SNM free 8T SRAM cell. This cell provides 2-3X times better read SNM even at lower voltages as shown in Figure2 [6].

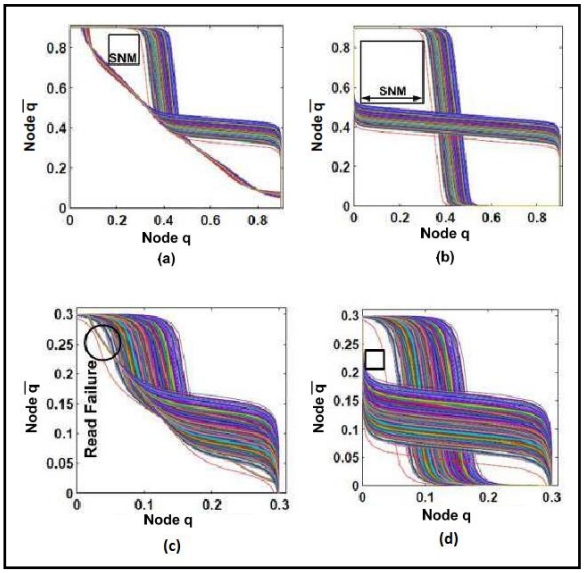


Fig 2 : (Above)Measurement of read static noise margin (SNM) at VDD =0.9V for 45nm technology node (a) standard 6T SRAM cell, and (b) read SNM free 8T SRAM cell. (Below) Measurement of read static noise margin (SNM) at V DD=0.3V for 45nm technology node (c) standard 6T SRAM cell, and (d) read SNM free 8T SRAM cell. [8]

*B. Current Mode Sense Amplifier*

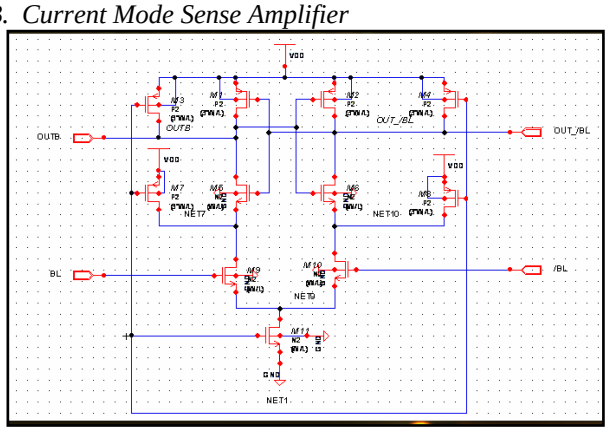


Fig 3: CMSA schematic circuit with 8T SRAM

Figure 3 shows the CMSA schematic circuit. The M9 and M10 are connected to BL and BL_Bar which is drives the transistors gate. For transistor M3, M4, M7 and M8 are the pre-charged transistors where the M1, M5 and M2 and M6 are the inverter pair cross coupled that resolves the BL differential voltage. Traditionally, this topology has been used because the memory bitlines are driving high impedance (gate) and full discharge of array bitline due to timing mismatch is not a concern [7]. The output of OutB and Out_/Bl is connected into inverters that convert the voltage differential at their inputs on BL and BL_Bar to a full swing at the output.

The operation of this sense amplifier design is based on the current differential that produced by M9 and M10 in the two pull down branches of this sense amplifier. During the read operation, when the BL or BL_Bar is low depending on the data stored in the cell. At the gate M11 is connected input pin Sense enable (SE), and when it set to low, it will automatically ON and the all the precharged transistors simultaneously turned off. Since the gate voltage of M9 and M10 differs by the generated bitline differential,

their channel currents are unequal. Thus the current that flow in M9 and M10 is unequal and it makes the voltage in either OutB or Out_/BL fall faster other than the other node. Therefore, this voltage is resolved by the cross-coupled inverters.

### C. *Voltage Mode Sense Amplifier*

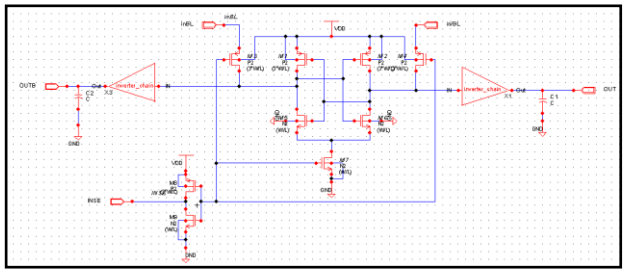

Fig 4: VMSA schematic circuit with 8T SRAM

Figure 4 above is the schematic of voltage mode sense amplifier. There are also two cross-coupled inverters in this design where M1, M5, and M2, M6 that resolve the differential voltage on the bitlines to a full swing at the output OUTB and OUT. The obvious advantage of this topology over the CMSA is the lower number od transistors needed which means faster access and smaller footprint [7].

The operation of this circuit is directly based on the voltage differential developed on its internal nodes by the input bitlines inBL and in/BL. At the output of the circuit is connected with inverter chain so that it gives the good output swing waveform. When the wordline in 8T SRAM is ON, M7 will turning off and let the M3 and M4 turn ON. At the gate terminal M7 is connected the input sense enable (SE) so that the cross-couples inverters amplifies this differential voltage to its output swing.

## III. DESIGN METHODOLOGY

### A. *Schematic*

The simulation of this design is by using Gateway SILVACO Tool. And the process technology is 0.18um. The first step in designing the circuit is to design the 8T SRAM circuit. To decide the width and length for the design, we must run the simulation and check the voltage transfer curve (VTC) if it is symmetry or not. We calculate the sizing based on the ratio of inverter which is 3:1. Figure below shows the VTC waveform of 8T SRAM with Vdd= 5V and the input is set varies from 0V until 5V. And we can see that the Vm point is symmetry where the value is 2.4471V and approximately to 2.5V and shows that the design is a good design and the sizing of W/L of the design is accepted. Thus the sizing of the PMOS and NMOS is show as the table1 below. The sizing of PMOS is 3 times larger than NMOS.

Table 1: Sizing of the transistors

| TRANSISTOR | SIZING W/L (um) |
|---|---|
| PMOS | 3*W/L = 60/1 |
| NMOS | W/L = 20/1 |

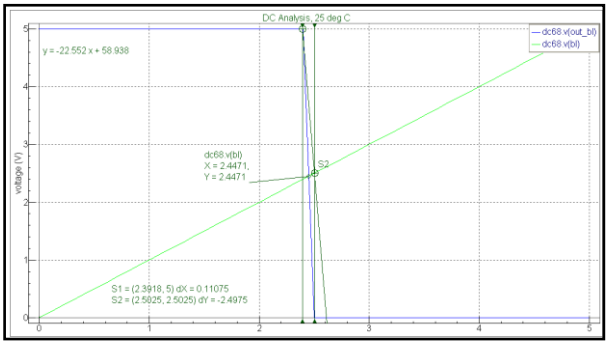


Fig 5 : VTC curve of 8T SRAM

After deicide the sizing of the transistors, next step is to design the sense amplifier for current mode and voltage mode. The sizing of these sense amplifiers are also same as the table x above. After finished drawing the schematic, we check the design rules if there is an error or not. If there is an error, it will not run the simulation. If there is error detected, than fix the error immediately. When the DRC shows no error, therefore we can run the simulation. Before proceed the simulation, we must set the control file of the design. Control file is used to put all the parameters that we have in the design such as the sizing W/L, temperature and also the library of the level simulation which is bsim3v3 level. All the data reading and taken during the simulation.

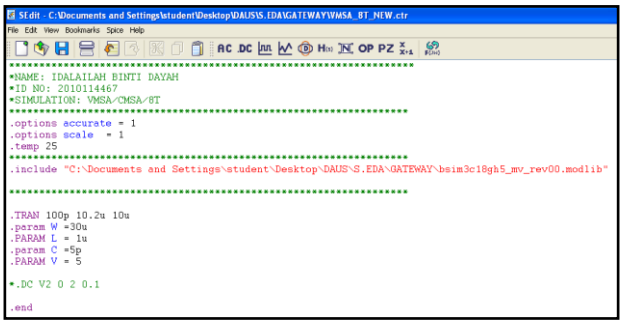


Fig6: Control File

In addition, we must create the symbol for each one of the circuit so that the design of 8T and the sense amplifier is simple and neat and easy to do run the simulation with different parameters. The symbol circuit can be seen in figure 7.

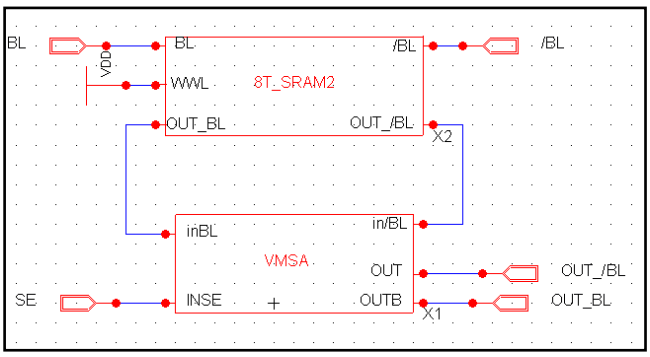


Fig 7: Symbol of 8T SRAM with VMSA.

### B. *Layout*

The software that we are used to design the layout is by using Layout Expert SILVACO Tool. The process technology that we are used is 0.18um which is from SILTERRA. Firstly, we create a new project so that we can save all the work that had done. After that, create a new cell for the different PMOS and NMOS so that easy to draw them and based on their sizing which is 60/1 and 20/1 for PMOS and NMOS. For length size, it represents the poly width. And for the width (W), it is representing by the height of the island. Save all the work done. After that, do the DRC check to identify the error. Next is to do the LVS which is layout versus schematic. In this section, we must get the layout and the schematic equivalent so that we know that our schematic is same as the layout design. Guardian LVS in EDA Tools is used for LVS checking. It recognizes the drawn shapes of layout as well as a connection between them.

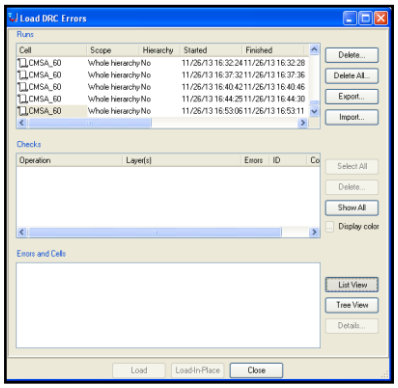

Fig 8: DRC report of CMSA.

## IV. SIMULATION RESULT AND DISCUSSIONS

### A. *Speed of operation*

CMSA is well known for the high-speed circuit for SRAM. Based on table 2 below, we can see the different value of delay that occurred between CMSA and VMSA where the Vdd is varied and the capacitance load is set to 5pF. When Vdd= 2V, the delay of VMSA is 64.46% larger than the CMSA which is 35.54% where VMSA is 12.4432nS and the CMSA is 6.8598nS. But as the number of Vdd increasing, the delay is decreasing. Still the VMSA has the larger delay compared to the CMSA. Thus, CMSA has the better speed compared to VMSA. The waveform of the delay is shows in figure 9 and 10.

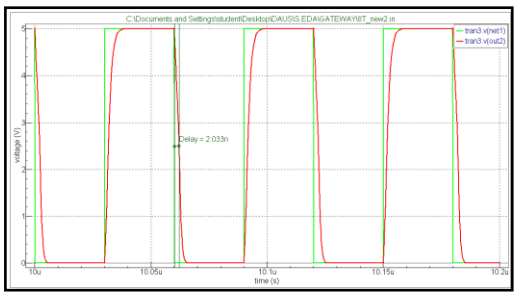

Fig 9: Output Delay 8T SRAM Vdd= 5V, CL= 5pF

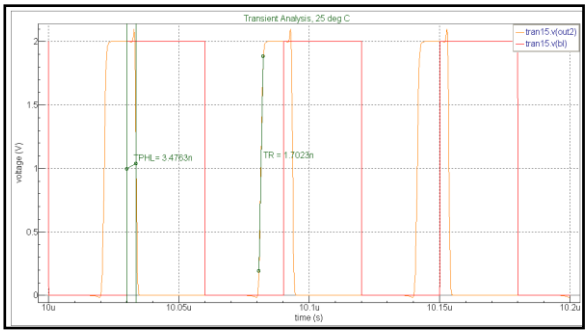

Fig 10: Propagation delay of VMSA by using Vdd=2V, CL= 5pF

TABLE 2: DELAY BY USING CL= 5pF

| | VMSA | | CMSA | |
|---|---|---|---|---|
| **VDD (V)** | **Delay (S)** | **%** | **Delay (S)** | **%** |
| 2 | 12.4432n | 64.46% | 6.8598n | 35.54% |
| 2.5 | 5.3948n | 52.33% | 4.91425n | 47.67% |
| 3 | 3.9399n | 51.51% | 3.70915n | 48.49% |
| 3.3 | 3.49395n | 51.25% | 3.3228n | 48.75% |
| 4 | 3.4286n | 55.48% | 2.75075n | 44.51% |
| 4.5 | 3.0235n | 54.77% | 2.49695n | 45.23% |
| 5 | 2.7546n | 54.36% | 2.3129n | 45.64% |

### B. *Current Dissipation*

By using the level3 library of Gateway SILVACO, the current dissipation ($I_D$) output value is shows in table 3 below. The value of Vdd is varied from 2V until 5V and the load capacitance is set to 5pF. The simulation for current dissipation is measured at the output of the sense amplifier. And the results show that the CMSA has the very small amount of current dissipation. In this design, the smallest current dissipation is the best. The leakage profile of the sense amp is also analyzed to identify transistor channel length and threshold voltage types that can be modified to improve the leakage power consumption of the design [1]. For Vdd=2V, $I_D$ for CMSA is 0.97387uA and VMSA is 5.77075uA which is 85.56% larger than CMSA, 14.44%. And during Vdd= 5V, the value is 6.32095uA (5.20%) for CMSA and 115.375uA (94.80%) for VMSA and the result is increasing as the voltage increasing. So, CMSA has the best current dissipation where its current dissipation is below to 15% compared to VMSA.

TABLE 3: CURRENT DISSIPATION BY USING CL= 5pF

| | VMSA | | CMSA | |
|---|---|---|---|---|
| **VDD (V)** | **ID (A)** | **%** | **ID (A)** | **%** |
| 2 | 5.77075u | 85.56% | 0.97387u | 14.44% |
| 2.5 | 4.05235u | 93.71% | 0.27204u | 6.29% |
| 3 | 18.6624u | 86.60% | 2.888445u | 13.40% |
| 3.3 | 62.4795u | 93.93% | 4.0361u | 6.07% |
| 4 | 75.855u | 95.68% | 3.42105u | 4.32% |
| 4.5 | 117.693u | 94.14% | 7.3264u | 5.86% |
| 5 | 115.375u | 94.80% | 6.32095u | 5.20% |

Table 4 below shows the power dissipation of both sense amplifiers and its percentage. At point B (current dissipation) above shows that the CMSA has the best current dissipation. Therefore, it is also same with power dissipation where CMSA has the less power dissipation compared to VMSA. The calculation of power dissipation is P= $I_D$V and the value of ID is taken from table 3 and times with Vdd.

TABLE 4: POWER DISSIPATION BY USING CL= 5pF

| | VMSA | | CMSA | |
|---|---|---|---|---|
| **VDD (V)** | **Power dissipation (uW)** | **%** | **Power dissipation (uW)** | **%** |
| 2 | 11.542 | 85.56% | 1.948 | 14.44% |
| 2.5 | 10.131 | 93.71% | 0.68 | 6.29% |
| 3 | 55.987 | 86.59% | 8.665 | 13.40% |
| 3.3 | 206.182 | 93.93% | 13.319 | 6.07% |
| 4 | 303.42 | 5.68% | 13.684 | 4.32% |
| 4.5 | 529.618 | 94.14% | 32.969 | 5.86% |
| 5 | 576.875 | 94.80% | 31.625 | 5.20% |

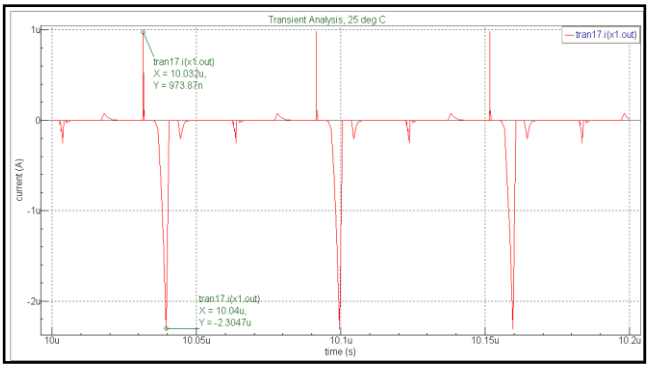


Fig 11: Current dissipation waveform of CMSA.

## C. *Noise Margin*

Table 5 below shows the Vin and Vo of high and low voltage for both sense amplifiers. The parameter is calculated by using Vdd 4.5V and 5V. And for table6, it shows the noise margin of both CMSA and VMSA sense amplifiers. During Vdd= 4.5, the NML of VMSA is higher than CMSA but for noise margin at high input, CMSA is greater than VMSA which is 50.05% and 49.95%. When Vdd=5V, the differences between these two noise margin can be seen that the VMSA has the higher noise margin compared CMSA, 65.54% and 34.46% for low voltage. It is because, the VMSA circuit is connected into inverter chain at the output, therefore it cause the current flow is through the output become slow and had to drive it for a long distance compared to the CMSA where it is just connected into the inverter. Therefore, it will caused the VMSA has the large noise margin and it is not good for this design. Thus, CMSA is a good design because of it as a low noise margin. Figure 12 shows the voltage transfer curve (VTC) of noise margin.

Table 5: Vin and Vo high and low for both SA

| VDD (V) | Symbol | VMSA | CMSA |
|---|---|---|---|
| 4.5 | VIL | 2.1934 | 2.1979 |
| | VIH | 2.3021 | 2.2976 |
| | VOL | 2.3021 | 2.2976 |
| | VOH | 4.5 | 4.5 |
| 5.0 | VIL | 2.2918 | 2.5931 |
| | VIH | 2.5025 | 2.7039 |
| | VOL | 2.5025 | 2.7039 |
| | VOH | 5 | 5 |

Table 6: Noise Margin of both SA

| VDD (V) | NM | VMSA | | CMSA | |
|---|---|---|---|---|---|
| 4.5 | NML | 0.1087 | 52.16% | 0.0997 | 47.84% |
| | NMH | 2.1979 | 49.95% | 2.2024 | 50.05% |
| 5 | NML | 0.2107 | 65.54% | 0.1108 | 34.46% |
| | NMH | 2.4975 | 52.10% | 2.2961 | 47.90% |

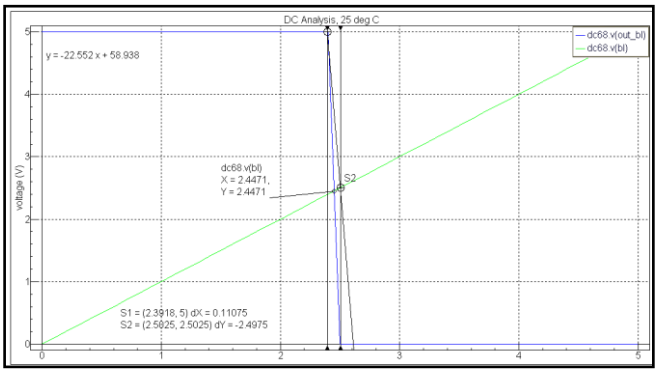


Fig12: VTC Noise Margin at Vdd=5V.

## D. *Area*

Figure 13 and 14 show the layouts for the CMSA and VMSA designs respectively. And figure15 is for 8T SRAM. The transistor area for the VMSA design is 30.98% less as compared to the CLSA design. The transistors that form the inverter pair in each sense-amp are also shown in the figure. Since the VMSA is known of its simplicity of circuit, thus it has the small area of layout compared to CMSA where 69.02% larger than VMSA. The report of LVS is also shown in figure 15 and 16. We can see the total nets and total devices that we are used in both schematic and layout.

Table5: Cell area of layout

| VMSA | | CMSA | |
|---|---|---|---|
| 39.015 x 89.17 um | 30.98% | 67.6 x 114.645 um | 69.02% |

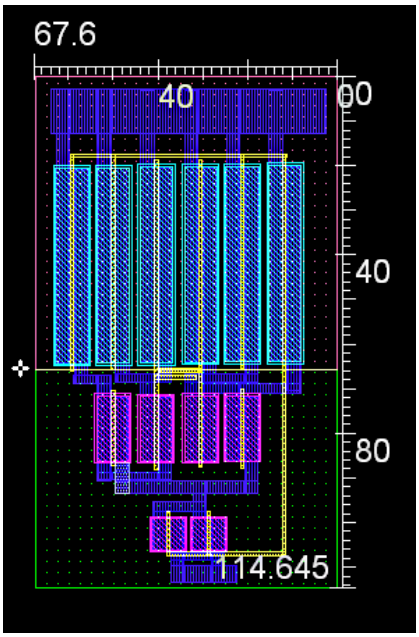


Fig 13: Layout of CMSA

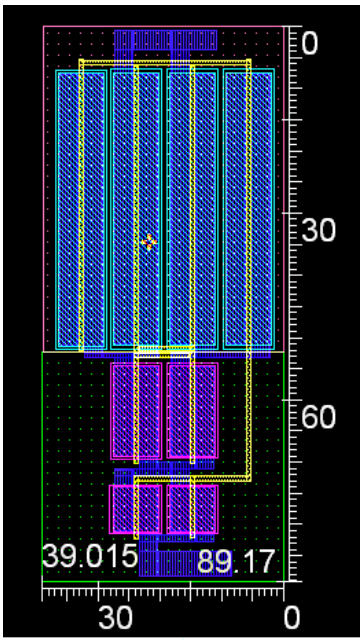


Fig 14: Layout of VMSA

Figure13 shows the layout of CMSA. On the top is PMOS and at the bottom is NMOS. Vdd is located on the top of PMOS while Vss is located at the bottom of NMOS. The input BL and BL_Bar is at the left and right of the NMOS which is at the gate terminal of the poly (yellow). At the bottom of the NMOS, it is M11 of the schematic. There are some techniques to get a good layout design. The layout using fingering transistor and try to makes the PMOS and NMOS same length so that the size of width or length can be reduce. Instead of using many metals in a layout design, the metals used can be reduce by apply the techniques of horizontal and vertical. It is also same with VMSA at figure14. The NMOS M7 is used the fingering technique. For figure14, PMOS at the top is using this technique so that it same as the size of the NMOS at the bottom.

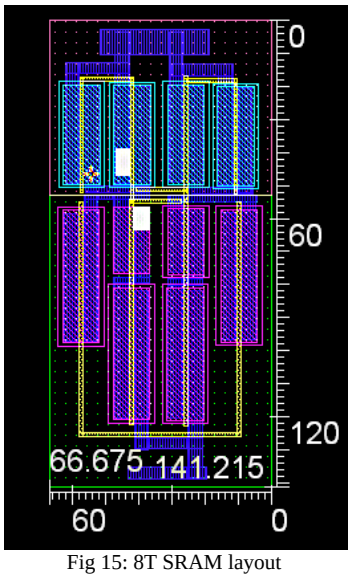


Fig 15: 8T SRAM layout

After finish draw the layout, the next step is should do the DRC which is design rules check for layout from SILTERRA. This DRC is used to check whether the design has the error or not so that it compatible to do the fabrication process. The DRC level for this design is successful with no error as shows in figure8. Figure16 and 17 below shows the LVS results for both sense amplifiers. LVS is stand for layout versus schematic to check if the layout and the schematic is equivalent with each other or not. Thus, the results for both shows the netlists are equivalent.

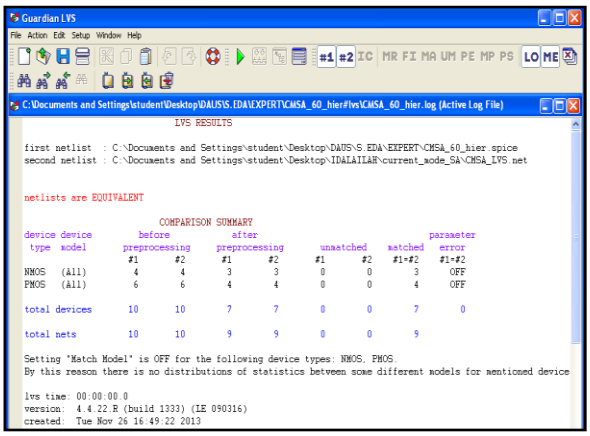


Fig16: LVS report for CMSA

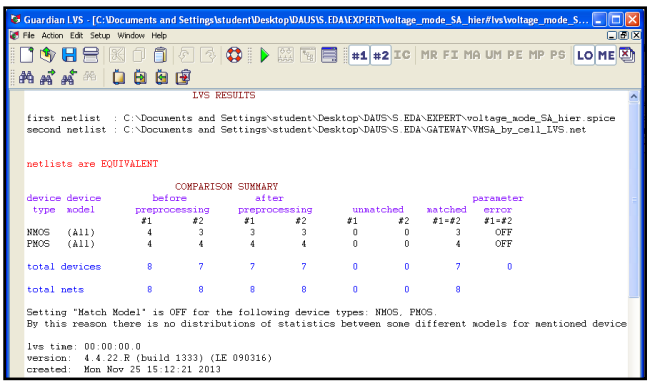


Fig 17: LVS report for VMSA

## V. CONCLUSION

This paper describes the simulation methodology used to compare the two VMSA and CMSA sense amplifier designs by using 8T SRAM. Therefore, the current-mode sense amplifier is better than the voltage-mode sense amplifier because the speed of current-mode is faster than voltage-mode where current mode is 36-46% less delay compares to voltage mode SA and it also has the small noise margin which is 35-50% less than VMSA. In addition, current mode has the small current dissipation which is it has 5-15% and the power dissipation is also less compared to the voltage mode sense amplifier. But, voltage mode also has its own specialty where it is 30.98% has small area less than current mode SA since voltage mode is known as the simplicity of the circuit. The simulations results clearly show the advantage of the CMSA design over the VMSA design. The faster speed of operation by the CMSA design makes it an ideal choice for high speed, low power data-path design. Thus, 8T SRAM is most efficient area since only view of transistors are used in the circuit. In view of the above, it can be concluded that the new SA is best suited for applications where low-voltage, low-power, high-speed and stability are of crucial design considerations.

## VI. RECOMMENDATION

In the future, we hope that we can compare any others type of sense amplifier and used different type of SRAM such as 6T, 7T, 9T and 10T. Other than that, we can use other software to do the simulation and different process technology so that we can get the good result and output for industry.

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## REFERENCES

[1] N. Dist, “Analysis of New Current Mode Sense Amplifier,” pp. 1–6.

[2] J. Zhu, N. Bai, and J. Wu, “A Review of Sense Amplifiers for Static Random Access Memory,” vol. 30, no. 1, 2013.

[3] A. V Gayatri, “Efficient Current Mode Sense Amplifier for Low Power SRAM,” vol. 1, no. 2, pp. 147–153, 2011.

[4] N. Verma, S. Member, and A. P. Chandrakasan, “A 256 kb 65 nm 8T Subthreshold SRAM Employing Sense-Amplifier Redundancy,” vol. 43, no. 1, pp. 141–149, 2008.

[5] J. Wang and H. Lee, “New Current-Mode Sense Amplifier for Low-Voltage Low-Power SRAM Design,” pp. 1–5.

[6] J. Singh and B. Raj, “SRAM Cells for Embedded Systems,” 2014.

[7] B. Mohammad, P. Dadabhoy, K. Lin, and P. Bassett, “Comparative study of current mode and voltage mode sense amplifier used for 28nm SRAM,” *2012 24th Int. Conf. Microelectron.*, no. Icm, pp. 1–6, Dec. 2012.

[8] P. Y. Chiang, “Sense amplifier power and delay characterization for operation under low-Vdd and low-voltage clock swing,” *2009 IEEE Int. Symp. Circuits Syst.*, pp. 181–184, May 2009.

[9] A.-T. Do, Z.-H. Kong, K.-S. Yeo, and J. Y. S. Low, “Design and Sensitivity Analysis of a New Current-Mode Sense Amplifier for Low-Power SRAM,” *Ieee Trans. Very Large Scale Integr. Vlsi Syst.*, vol. 19, no. 2, pp. 196–204, 2011.

[10] S. K. Jain and P. Agarwal, “A low leakage and SNM free SRAM cell design in deep sub micron CMOS technology,” *19th Int. Conf. VLSI Des. held jointly with 5th Int. Conf. Embed. Syst. Des.*, p. 4 pp., 2006.

[11] G. V. Kristovski and Y. L. Pogrebnoy, “New sense amplifier for small-swing CMOS logic circuits,” *IEEE Trans. Circuits Syst. II Analog Digit. Signal Process.*, vol. 47, no. 6, pp. 573–576, Jun. 2000.

[13] M. Sinha, S. Hsu, a Alvandpour, W. Burleson, R. Krishnamurthy, and S. Borkar, “High-performance and low-voltage sense-amplifier techniques for sub-90nm SRAM,” *IEEE Int. Syst. SOC Conf. 2003 Proc.*, pp. 113–116, 2003.