Analysis And Design of a Low Power, High Speed Sample And Hold Circuit for Pipelined ADC Using 0.18µm CMOS Technology

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***Abstract*—This paper present an analysis and design of Sample and Hold (SH) circuit for front end block pipelined ADC using 0.18µm CMOS technology. The objective of this project is to design a sample and hold circuit and analyzing in term of low power and high speed with two different topologies, which are two stage operational amplifier and folded cascode operational amplifier. The analysis of op amp parameters is done for 0.18µm CMOS technology. SILVACO EDA tools have been used for schematic design and simulation. Complete sample and hold circuit has been designed with 1.8V Vpp, 1.8V voltage supply, and 5MHz sampling frequency. The power consumption for two stage operatinal amplifiers is 0.081mW and 0.593mW for folded cascode operational amplifier. The propagation delay of the circuit is 131.15ns for two stage operational amplifier and 2.7402ns for folded cascode operational amplifier. Based on the analysis and design, two stage operatinal amplifier can give low power consumption and low speed while folded cascode operational amplifier give high power consumption but high speed.**

Keywords-component; Sample and Hold circuit; ADC; operational amplifier.

I. INTRODUCTION

With the demand for pipelined Analog Digital Converter (ADC) has increased rapidly with the growth of technology [1], with having various advantages including as an alternative solution for wireless communication system, the performance of Sample and Hold (SH) circuit in pipelined ADC will take into consideration as the SH circuit play the main part in the ADC which the performance of the SH circuit will affect the whole ADC [2] . In other hand, power consumption and speed of the SH circuit will be the main focus during the circuit design as these two factors has become the major problem and typically the pipelined analog to digital converter are used for the applications that requires low power and high speed.

The SH circuit in pipelined ADC mainly begins with the conversion process which place in front of the ADC. The operations of the SH block consist of two phases, the sampling phase and the hold phase [3]. For sampling phases, the analog signal is sampled in capacitor whereas the SH circuit works as buffer. In holding phase, the analog sampled signal will keep fixed until the next sampling phase, whereas the SH circuit will allow the voltage comparison of the signal, thus determine the function of the SH block itself where the SH circuit is to sample an analog input signal and hold the value over a certain length of time for subsequent processing.

The software used in this project is SILVACO EDA tool by using 0.18µm CMOS technology. SILVACO delivers a comprehensive set of leading edge TCAD and EDA tools. The SILVACO EDA Gateway tool is used to design a schematic and support flat or hierarchical designs of any technology. The advantages of using Gateway is, it can be used by large design teams through global preferences and handles multiple designs and technologies with specific workspaces.

A. Project Objective

The objective of this paper is to analyze in term of power consumption and speed of the sample and hold circuit for various approaches in different type of op amp which is two stage operatinal amplifier and folded cascode operational amplifier. Thus, the main application of this sample and hold circuit is in the low power and high speed pipelined ADC. Circuit has been designed in 0.18µm CMOS technology.

B. Project Overview

The sample and hold architecture has been designed in SILVACO EDA tool. Different topologies have been designed in order to analyze the characteristic of the sample and hold circuit in term of low power and speed of the design. Two different topologies which are two stage operational amplifier and folded cascode operational amplifier has been used in this design. Analysis on the result obtained was discussed.

C. Scope of Work

The analysis of the sample and hold architecture design has been done in SILVACO EDA tool. The schematic of the circuit was design in SILVACO Gateway and the result of the

circuit has been simulated in SILVACO Smartspice. This paper has divided into four sections. Section II describes the literature review of the project, section III describe project methodology which includes project architecture and design procedure. Result and discussion will be discuss in section IV while the conclusion on sample and hold circuit for pipelined ADC will be conclude in section V.

II. LITERATURE REVIEW

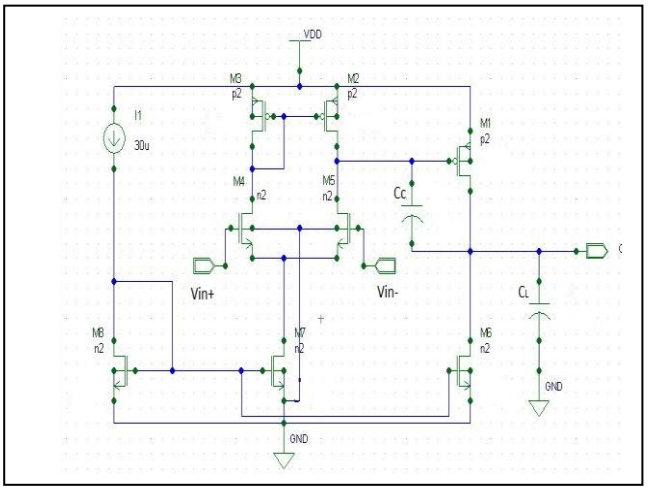

Figure 1: Two stage operational amplifier circuit

The two stage operational amplifier circuit has shown in Figure 1. The two stage operational amplifier circuit is most common and widely used as its performance closely meet the design specifications. The differential amplier consist in the first stage of the circuit which will convert the differential input voltage to differential current. The differential current then are applied to the current mirror load. Second stage of the circuit consist of common source MOSFET that will converting the second stage input voltage to current. The first stage of the circuit will increase the DC gain by an order of magnitude and maximizes the output signal swing at the second stage thus reducing the power consumption [4].

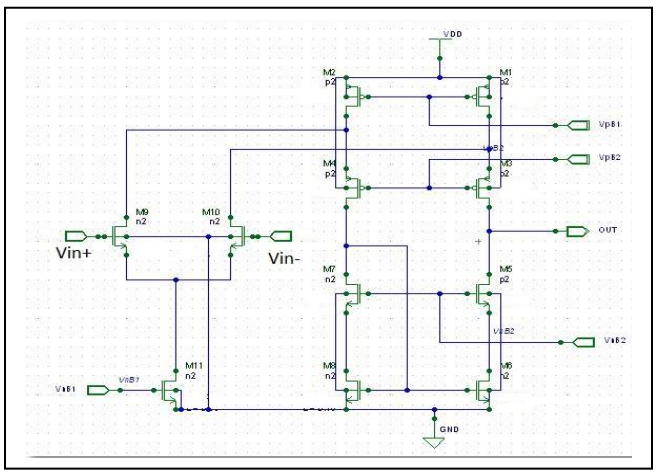

Figure 2: Folded cascode operational amplifier circuit

Figure 2 above shows CMOS folded cascode operational amplifier circuit which will be used in designing the sample and hold circuit. The folded cascode circuit widely used in switched capacitor circuit due to higher power supply rejection ratio and provide higher frequency operation than the two stage operational amplifier. The comparison between these two circuit topology will be discuss on the design behavariour.

Both of the topologies then will be implement in the sample and hold circuit. The storage element and a switch are the two basic elements for sample and hold circuit [5]. The capacitor will implemented as storing element and the MOSFET for sampling element. Figure 3 below shown the schematic of the sample and hold circuit.

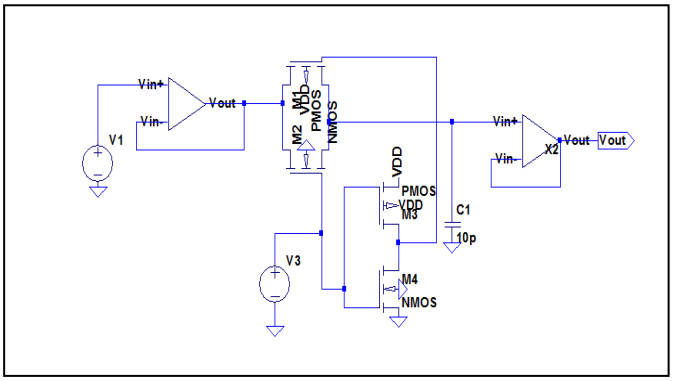

Figure 3: Schematic of sample and hold circuit

The transmission gate, Tx will be placed in the sample and hold circuit to pass the positive and negative voltages of MOSFET. The Tx gate will ON the resistance of the switch thus will determine the RC time constant to charge the capacitor. Two operational amplier are used as buffer to avoid the loading effect on the soure when sampling and to avoid the discharge through the capacitor when it is in hold mode.

III. METHODOLOGY

Figure 4 below shows the block diagram of the pipelined ADC. It is consist of sample and hold circuit in part of the block diagram. The sample and hold circuit is the front end block of the pipelined ADC which including the operational amplifier and few other elements.

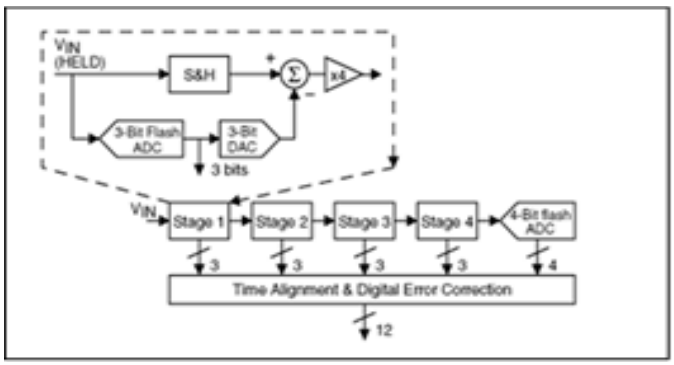

Figure 4: Block diagram of pipelined ADC

Sample and hold circuit is an important analog building block with many applications, including pipeline ADC and switched capacitor filters. The function of the SH circuit is to sample an analog input signal and hold this value over a certain length of time for subsequent processing.

The increasing popularity of digital signal processing in high frequency applications requires the development of high performance analog to digital converters. Compared with other ADC, pipelined ADC has the advantages of high speed, high precision and low power consumption, so pipelined ADC has become an important structure in the high speed low power applications. Speed and precision of a close loop sample and hold circuit primarily depends on the performance of the op amp used, so special care has been taken to meet the requirement of the op amp DC gain, bandwidth, slew rate and settling time, etc. The use of sample and hold circuit allows most non-linear effects of ADC to be reduced especially those occurring with high frequency input signals [3]. So the SH circuit must do better performance than the other parts of the ADC, including a wider bandwidth, the ability to drive the large load with low distortion, less additional noise and low power dissipation.

Flow chart in Figure 5 shows the project steps in order to complete the low power and high speed design of sample and hold circuit using SILVACO EDA TOOLS software with 0.18µm CMOS technology. The parameters of the transistor sizing will be determine and specific in order to analyze the behavior of the design circuit. Folded cascode operational amplifier and two stages operational amplifier has been design.

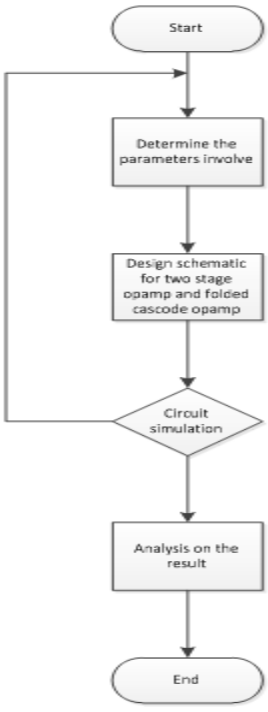

Figure 5: Flow chart of the project step

From the flowchart above, the first step is to determine the specification of this project. In the other hand, the specification is the important thing to achieve to make sure the project is successful. When the specification has been decide, the next step is to design a schematic. The schematic for SH circuit with different type of operational amplifier which are folded cascode operational amplifier and two stage operational amplifier. The software used for design the circuit is SILVACO EDA Gateway tool. The schematic then simulated using Smartspice simulator and the result then will be analyze.

IV. Result and Discussion

The circuit for sample and hold is simulated and the result is summarized in table 1. There are three part of the design that will discuss, first part is power consumption, the second part is the speed of sample and hold circuit design and the third part is simulation on sample and hold circuit design.

TABLE I. COMPARISON OF PERFORMANCE FOR TWO STAGE AND FOLDED CASCODE OP AMP

Type of Op Amp	***Technology***	***Power Consumption***	***Delay***
Two Stage	0.18µm	50.30mW	614.63ns
Folded Cascode	0.18µm	65.67mW	32.865ns

Based on the result seen in TABLE I, the two stage operational amplifier results in higher delay which define the speed of the design is low compared to folded cascade operational amplifier whereas the propagation delay of the folded cascode operational amplifier is less than two stage operational amplifier which result the high speed design of the sample and hold circuit.

A. Speed

Other requirements that encounter in sample and hold circuit is high speed as in front block of pipelined analog to digital converter. The simulation results obtained for two stage operational amplifier and folded cascode operational amplifier shown in figure 6 and figure 7 respectively.

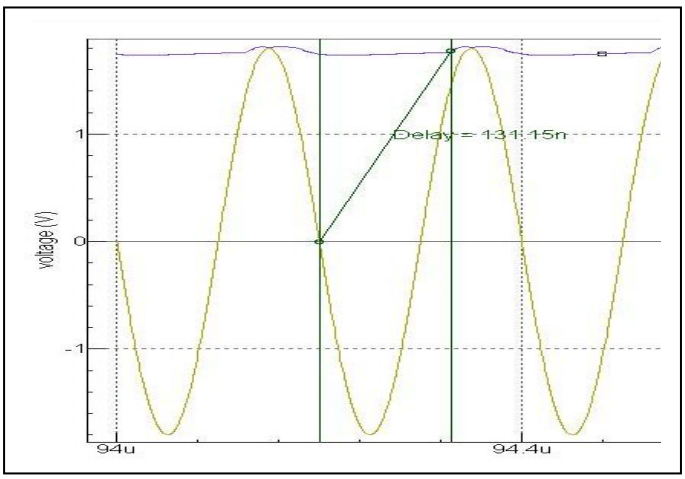

Figure 6: Simulation output for delay in two stage operational amplifier

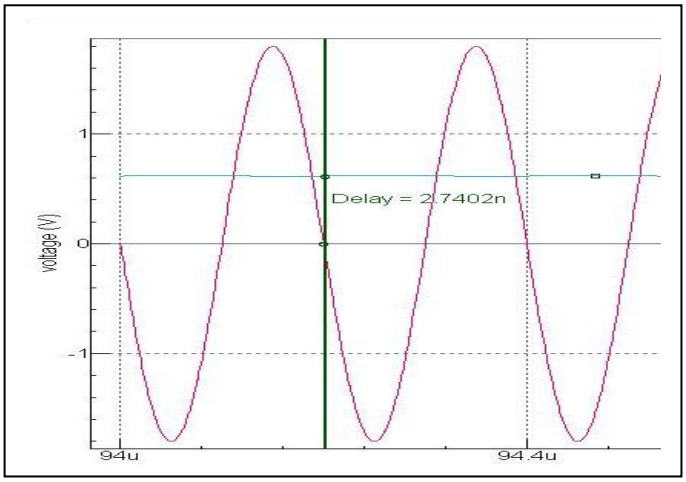

Figure 7: Simulation output for delay in folded cascode operational amplifier

Simulation result for two stage operational amplifier gives the value of 131.15ns and 2.7402ns for folded cascode operational amplifier which shows that folded cascode operational amplifier results in high speed of sample and hold circuit design.

B. Power Consumption

Power consumption has become major design consideration in digital CMOS Design. There are two important characteristic of CMOS design which is noise immunity and low static power consumption. The power consumption mainly driven the current trend towards low power mainly has driven by two forces such higher demand for long life autonomous portable equipment and technology. Therefore, the limitation of high performance of the system also effecting the current trend thus the power consumption. In simulation in term of power, the value of power measured in sample and hold circuit with different topologies including two stage operational amplifier and folded cascode by editing the SEdit in SILVACO EDA tools as shown in Figure 8 below.

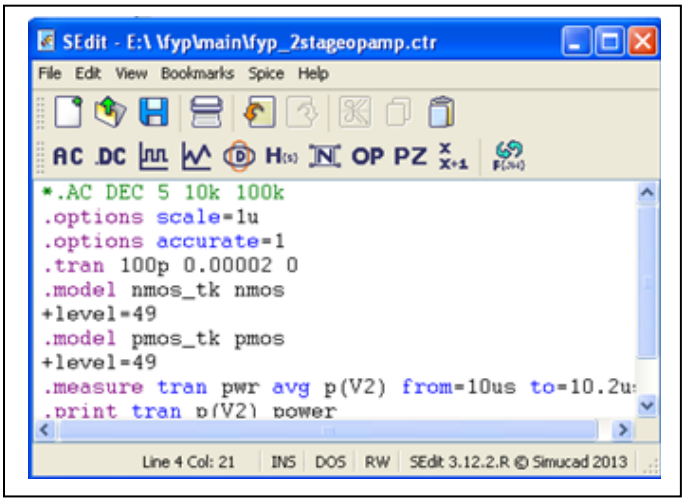

Figure 8: SEdit for power consumption measurement

The value of power obtained for different topologies was summarized in TABLE I. Based on the simulation result, folded cascode operational amplifier results in high power performance compared to two stage operational amplifier.

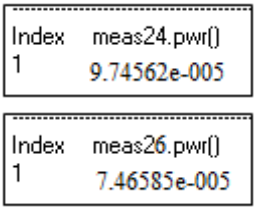

Figure 9: Results of power consumption for two stage and folded cascode op amp respectively

C. Average Dynamic Power Dissipation

In the circuit, the average dynamic power dissipation can be happen whe the capacitors is start to charging and discharging or overturn of inverter and latch. The simulation done in Gateway simulator with 0.18µm CMOS technology. As shown in simulation, the average dynamic power dissipation for two stage operational amplifier is 282.86µW and 598.58µW for folded cascode operational amplifier. The folded cascade operational amplifier gives high result than the two stage operational amplifier.

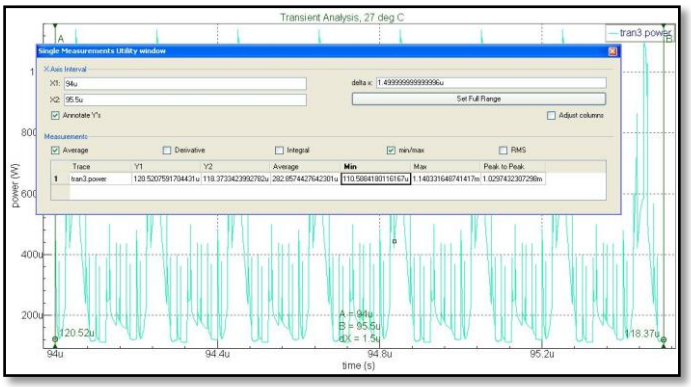

Figure 10: Average dynamic power dissipation for two stage opamp

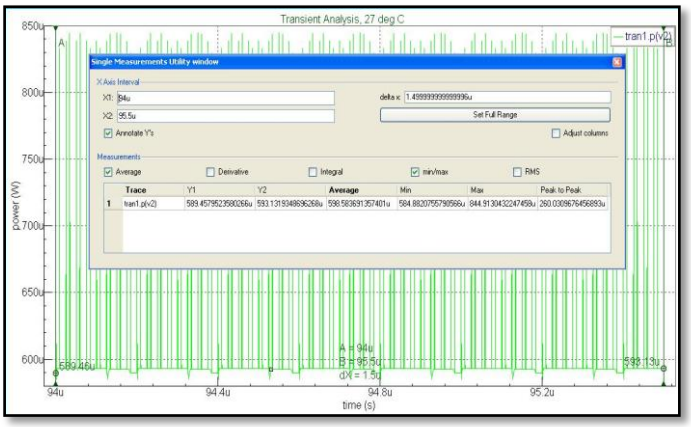

Figure 11: Average dynamic power dissipation for folded cascade opamp

D. Sample and Hold Circuit

Sample and hold circuit is an important analog building block with various applications. An example of sample and hold circuit shown in Figure 4 in which there are an input buffer, switch, and output buffer to sampled out the output. The sampling period is kept small as compared to holding period so that the output of the op amp will get settled. The simulation result for sample and hold circuit as shown in Figure 10 below. The figure shows the transient result of sample and hold circuit for output voltage. The simulation is done in 0.18µm CMOS technology with 1.8V voltage supply.

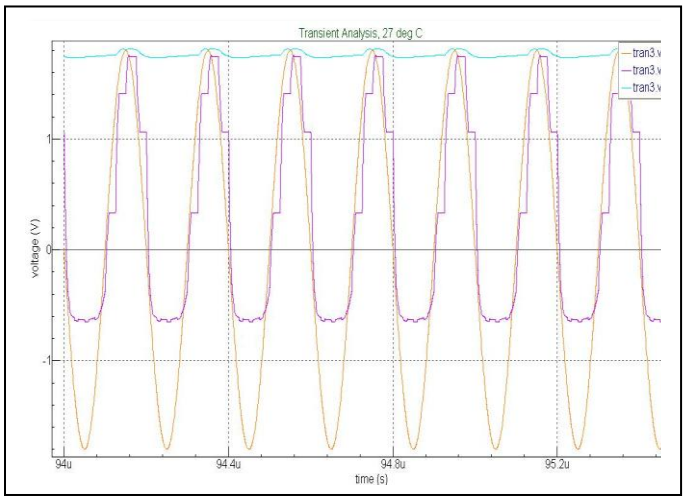

Figure 10: Simulation output for Vout of sample and hold circuit

V. CONCLUSION

This paper has presented an improved design technique for sample and hold circuits to be used in high-speed ADC with different topologies use in architecture which are two stage operational amplifier and folded cascode operational amplifier. The design is simulated using 0.18µm CMOS technology with 1.8V voltage supply for operating in low power. The simulation result for the two stage operational amplifier and folded cascode operational amplifier thus indicate that the two stage operational amplifier can give low power consumption and low speed while folded cascode operational amplifier give high power consumption but high speed. However, due to the several limitations, the actual output cannot be obtained due to some error in designing the sample and hold circuit as an expected.

VI. FUTURE DEVELOPMENT

For future development of work, the better and faster sample and hold circuit must be developed. The fastest of sample and hold circuit operate in open loop but the accuracy is low compared to sample and hold circuit operate in closed loop which can achieve high resolution in term of gain and speed [6] . Other than that, the analog circuits are now employed with voltage mode to current mode compared to the employment of low voltage in technology nowadays that required the circuit to be low as well. Therefore, future research should be also shift towards current mode sample and hold techniques.

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