Safe Commutation Studies for Single Phase Matrix Converter Operation as Inverter

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***Abstract* :- This paper presents safe commutation studies for switching strategy sequence of single-phase matrix converter (SPMC) operating as inverter modulated by the Sinusoidal Pulse Width Modulation (SPWM). The power circuit uses the Insulated Gate Bipolar Transistor (IGBT) as switching device in the SPMC implementation. The switching control sequence for safe-commutation strategies has been defined and implemented to solve switching transients with sample verification on results. A Xilinx Field Programmable Gate Array (FPGA) was used at the heart of the control electronics, implemented to verify operation. This is then modeled using a Matlab Simulink (MLS) and verified experimentally.**

***Keywords:* Sinusoidal Pulse Width Modulation (SPWM), Insulated Gate Bipolar Transistor (IGBT), Single-Phase Matrix Converter (SPMC), Matlab Simulink (MLS)**

I. INTRODUCTION

Many theoretical studies have been investigated on Matrix Converter (MC) but have found limited practical applications in power electronics. The matrix converter (MC) offers possible an "all silicon" solution for AC-AC conversion, removing the need for reactive energy storage components used in conventional converter system [1]. The topology was first proposed by Gyugyi [2] in 1976. The Single-phase Matrix Converter (SPMC) was first realised by Zuckerberger [3]. Other SPMC topology had been studied by Hossieni [4] and Abdollah Khoei [5]. All previous works have focussed attention to direct AC-AC single-phase converter [6]. Very few publications have been found on SPMC but none with commutation strategies in their implementations. This problem needs to be resolved in any Pulse Width Modulation (PWM) type of converters due to absence of natural freewheeling paths [7] as available in other traditional converter topologies.

The problem of commutation in SPMC occurs when inductive load is used. The use of PWM type of switching algorithm in SPMC will result with possible switching spikes being developed during switch turn-off or during commutation [8]. This paper describes the work involved on the implementation of SPMC as DC-AC inverter operation with subjected to the passive loads condition. Commutation problems due to the usage of inductive loads that arises the switching spikes are implemented with safe- commutation switching algorithm. The switching algorithm has been designed which allows all switches to take part in the safe-commutation strategy.

This paper will discuss the design and development of Sinusoidal Pulse-Width Modulation (SPWM) generator suitable for SPMC operating as inverter. It is based on the Xilinx chip XC4005XL FPGA with IGBTs as the power switching device. The output voltage is synthesized using Sinusoidal Pulse Width Modulation (SPWM). The proposed design enables the modulation index and the switching frequency to be changed externally. The experimental result from hardware implementation will be compared with those simulations using Matlab Simulink (MLS) to verify proposed operation.

II. SCOPE OF WORK

The scope of this project is to carry out the control of voltage spikes of DC-AC converter by using Single Phase Matrix Converter (SPMC) works in developing computer simulation models within the MATLAB/SIMULINK based on proposed switching strategies, to study the behavior. After that SPWM generator was developed as the switching technique for 5 kHz switching frequency to make SPMC as inverter operation using Xilinx Foundation software then compile and upload to Xilinx FPGA XC4005XL chip. This Xilinx FPGA was used as digital control implementations which can result current and voltage spikes were eliminated when inductive load was apply. The simulations result then compared with experimental result.

III. RESEARCH METHODOLOGY

Figure 1 below illustrates the research methodology adopted in investigation and implementation of this work. After done a literature review, there are three different main parts which is do simulation, design using Xilinx software and lastly test at hardware. In simulation part, MATLAB/Simulink was use as simulation tool to study the behavior of SPMC. After that continue with design SPWM generator using Xilinx foundation software then compile and upload to Xilinx XC4005XL chip. Lastly test using hardware that consist eight IGBT and Xilinx board. The test was conduct for with and without commutation strategy.

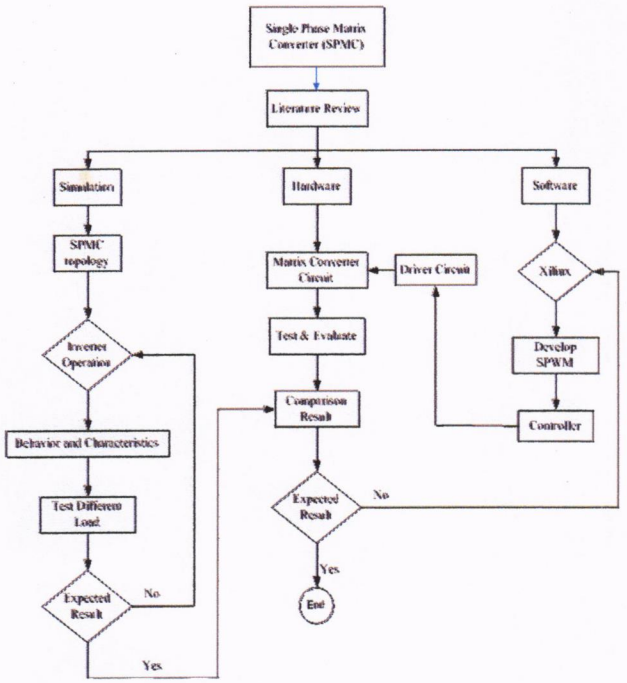


Fig. 1: Research methodology

IV. SINGLE PHASE MATRIX CONVERTER

The SPMC requires 4 bi-directional switches as shown in Fig. 2; each capable of conducting current in both directions, blocking forward and reverse voltages [9]. It requires the use of bidirectional switches capable of blocking voltage and conducting current in both directions. Unfortunately there is no discrete semiconductor device currently that could fulfill the needs [10, 11] and hence the use of common emitter anti-parallel IGBT, diode pair as shown in Fig. 3. The IGBT were used due to its popularity amongst researchers that could lead to high-power applications with reasonably fast switching frequency for fine control, whilst the diodes provides reverse blocking capabilities to the switch module. The new bi-directional switch module configuration can be observed from Fig. 3 whereby the left part is named as 'Switch a' and right part named as 'Switch b' which the direction of current flows is to be upward and downward respectively. This direction of current flows is applied to all switches. The overall SPMC circuit configuration can be seen from Fig. 4.

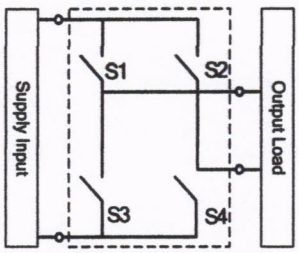


Fig. 2: Bi-directional Switch

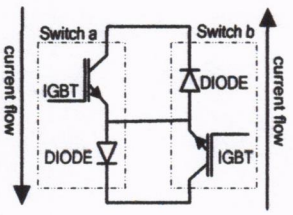


Fig. 3: Bi-directional switch module (common emitter configuration)

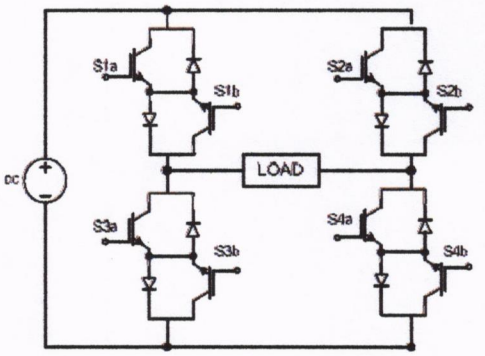


Fig. 4: SPMC circuit configuration

V. INVERTER OPERATION

The output waveforms of ideal inverters should be sinusoidal. However the waveforms of practical inverters are non-sinusoidal and contain certain harmonics. For low and mediumpower applications, square-wave or quasi-square-wave voltage may be acceptable: and for high-power applications, low distorted sinusoidal wave forms are required. With the highspeed power semiconductor devices the harmonic contents of output voltage can be minimized or reduced significantly by switching techniques.

The inverter proposed is presented schematically in Fig. 5 and Fig. 6 with various possible switching states defined in Table 1. However, since the SPMC is capable of conducting current in forward and reverse directions, it is also possible that the DC side becomes the generating source and the AC side becomes the receptacle. In this way the SPMC can function either as a voltage source inverter (VSI) or a current source inverter (CSI) supplying various shapes of alternating current to the AC supply system. These currents are then normally used for cancelling harmonic distortions in supply system and provide unity power factor operation.

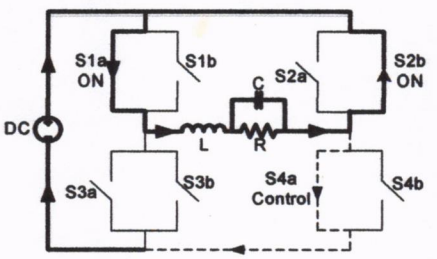


Fig. 5: State 1 (positive cycle)

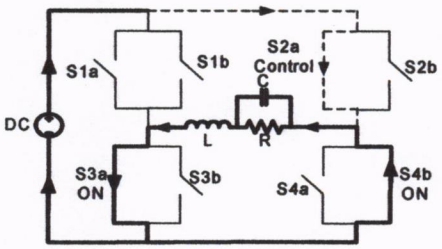


Fig 6: State 2 (negative cycle)

In Figure 5, the bold-line represents the current flow for commutation switches; S1a and S2b. The dotted line represents the control (SPWM) switch, S4a. Similar illustration is used in Fig. 6, the bold-line represents the current flow for commutation switches; S3a and S4b. The dotted line represents the control (SPWM) switch, S2a.

The well known SPWM used in power electronics are as illustrated in Fig. 7. A triangular carrier signal, V_c, is compared with a sinusoidal reference signal, V_{ref}, of the desired frequency. The crossover points are used to determine the switching instants.

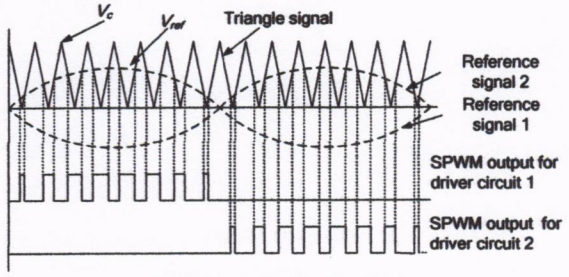


Figure 7: Formation of SPWM

The magnitude ratio of the reference signal (V_{ref}) to that of the triangular signal (V_c) is known as the modulation index (m_i). The magnitude of fundamental component of output voltage is proportional to m_i. The amplitude V_c of the triangular signal is generally kept constant. By varying the modulation index, the output voltage could be controlled.

$$m_i = \frac{V_c}{V_{ref}}$$

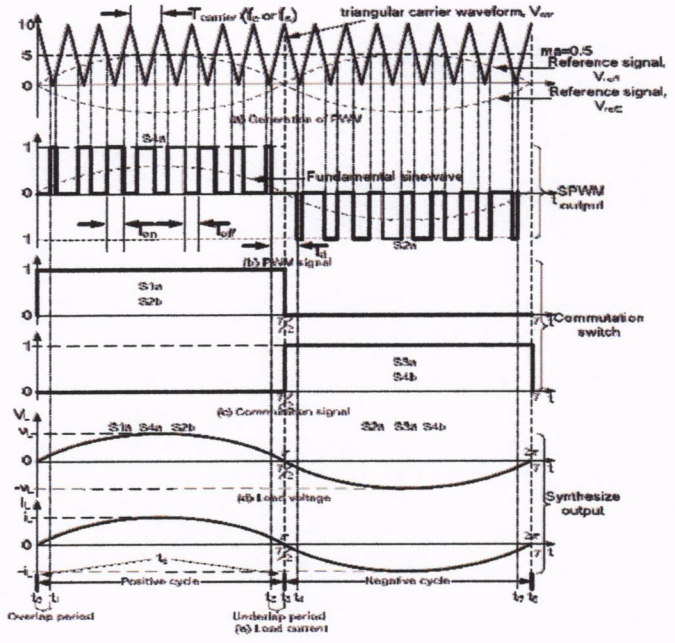


Fig. 8: Switching pattern of inverter, resistive load with LC filter

Fig. 8 shows one complete switching cycle (positive and negative cycle) is divided into six states described as follows;

Step 1: (t0~t1) at time t0, S1a and S2b are turned ON provided the overlap period prior to S4a being switched with PWM control.

Step 2: (t1~t2) at time t1, control (SPWM) switch S4a is turned ON (after delay time). During this period, current flows into the inductive load (energized) through S1a and left to be dissipated deenergized) through S2b when S4a is turned OFF.

Step 3: (t1~t2) at time t2, control (PWM) S4a is turned OFF and the inductive load is de-energized during underlap period between S4a and S2b being active.

Step 4: (t3~t4) at time t3, S3a and S4b are turned ON to provide an overlap period prior to S2a being switched with PWM control.

Step 5: (t4~t5) at time t4, control (SPWM) switch S2a is turned ON (after delay time). This operates in a similar manner to step 2.

Step 6: (t5~t6)at time t5, S2a is turned off. A complete switching cycle is ended to complete a switching cycle.

VI. COMMUTATION PROBLEM

In conventional converters, free-wheeling diodes are used for this purpose. In SPMC these free-wheeling diodes do not exist, hence switching sequence need to be developed to allow for energy to dissipate during commutation, thus protecting the converter from being damaged due to those spikes described.

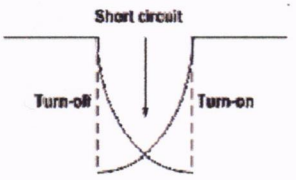


Figure 9 : Short circuit configuration in IGBT

Theoretically the switching sequence in the SPMC must be instantaneous and simultaneous; unfortunately impossible for practical realization due to the turn-off IGBT characteristic, where the tailing-off of the collector current will create a short circuit with the next switch turn-on. This problem arises when inductive loads are used. A change in current due to switch commutation and PWM switching will result in two damaging phenomena. First current spikes will be generated in the short-circuit path and secondly voltage spikes will be induced as a result of change in current direction across the inductance. Both will subject the switches with undue stress leading to destruction.

VII. COMMUTATION STRATEGY

The use of Sinusoidal Pulse Width Modulation (SPWM) is a well known wave shaping technique in power electronics as illustrated in Fig. 10, results with possible reversal voltage if inductive loads are used, during switch turn-off [12], restated here briefly for completeness.

Driver circuits are designed to generate the SPWM patterns that are used to control the power switches, comprising IGBTs in the SPMC circuit. The use of SPWM as the switching algorithm in this converter, results with possible reversal current if inductive loads are used, during switch turn-off. This technique will result with the existence of switching transients relating to the inductive load during switch turn-off.

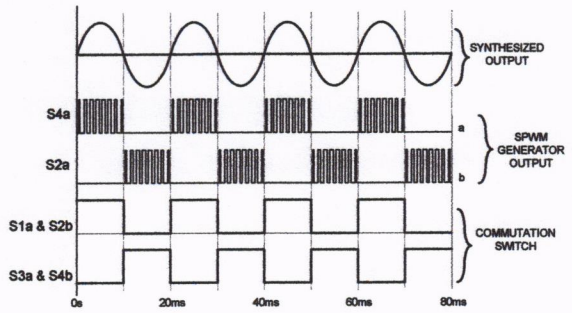


Fig 10: Switching Pattern for Commutation Strategy

In order to overcome these difficulties, safe-commutation strategy with switching sequences was defined and developed to prevent current and voltage spikes induced by manipulation of the switch according to the switching state in Table 1. By referring to Fig. 5, for state 1 (positive cycle), switch S4a is fed with SPWM signal, whilst S1a and S2b will be 'on' for positive state. During the positive cycle, the commutation switches that are used to afford the current path are provided by the upper-part switches i.e.; S1 & S2. This arrangement is similarly implemented for state 2 (negative cycle), where switch S2a is controlled by the SPWM signal, whilst S3a and S4b is turned 'on' for negative state as illustrated in Fig. 6. The switching strategy proposed is more systematic because it uses all the switches for providing the path of free-wheeling in avoiding the generation of voltage and current spikes.

Table 1: Switching strategies of Inverter

Switches	Operation	
	Positive Cycle (State 1)	Negative Cycle (State 2)
S1a	ON	OFF
S1b	OFF	OFF
S2a	OFF	CONTROL
S2b	ON	OFF
S3a	OFF	ON
S3b	OFF	OFF
S4a	CONTROL	OFF
S4b	OFF	ON

The switching sequence for operation of SPMC as an inverter for an output of 50Hz is tabulated in Table 1, with its switching sequence shown in Figs. 8 and 10 for an output frequency of 50 Hz.

VIII. SIMULATION AND MODELING

MATLAB Simulink (MLS) is used as simulation tool to study the behavior of the rectifier operation. Figure 11 shows the top level main model of the SPMC. The subsystems are as shown in Figure 12 through 14.

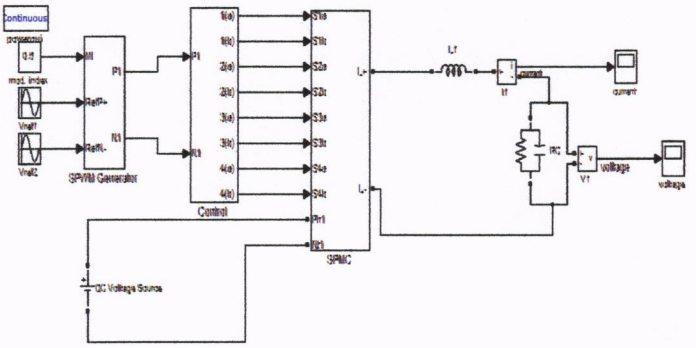
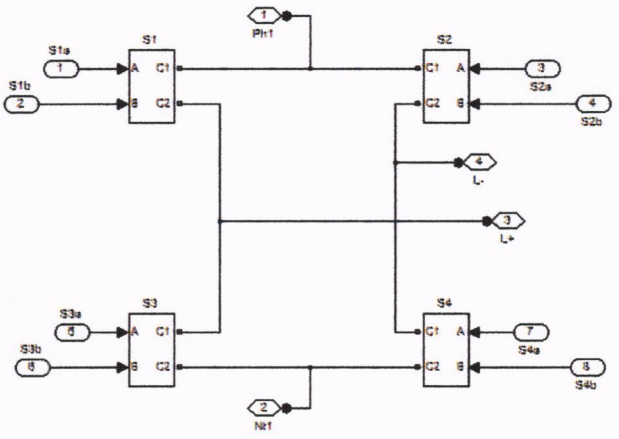
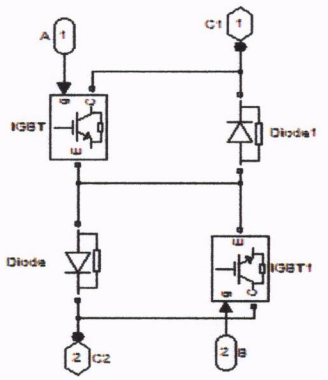


Figure 11: Top level main model of controlled rectifier



(a)



(b)

Figure 12: (a) SPMC Model in MLS and (b) Bidirectional switch module

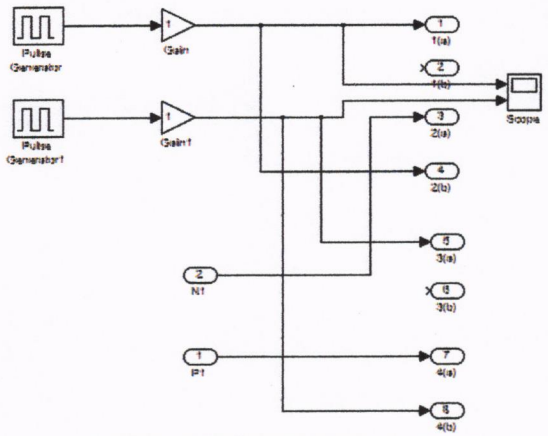


Figure 13: Controller unit for inverter

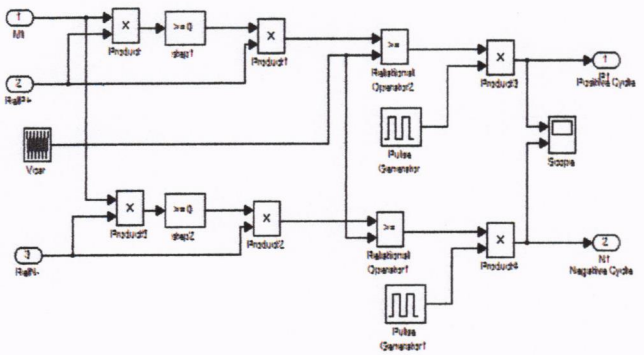


Figure 14: (a) SPWM generator model

The overall block diagram of the SPWM generator in FPGA is as shown in Fig. 15 and the top level XILINX schematic diagram is as shown in Fig.16. There are 7 major components, namely; 1) External Main Clock, 2) 'W' shape carrier signal, 3) Comparator, 4) Multiplier, 5) Modulation Index, 6) ROM and 7) Memory Pointer. Actually SPWM signal generate by comparing the triangular wave signal with the sinusoidal voltage reference signal which can be adjusted to get the Sinusoidal Pulse Width Modulation algorithm. An external main clock was used as the clocking signal for the FPGA counter. For this work, 5 KHz carrier signal was used. The 8 bit up-down counter, CB8CLED is clocked at 2.55MHz to produce 5 KHz carrier signal. The toggle flip-flop, FTC is used to counts and changes the counting direction of the up-down counter. The counter start counting from 0 to 255 when the reset signal, 'RST' is received and it will count back to 0. This process will produce 'M' shape carrier signal. The multiplier (MULTIPLY) block as shown is created using VHDL used to multiply the external source data (Modulation Index, MLTY) with the data stored in ROM (reference sine-wave). The modulation index is set by using 4-bit external data. The magnitude of sine-wave magnitude are obtained by multiplying the input from the external data. Inverter, INV8 was used to change 'M' shape to 'W' shape. This triangular 'W' shape then will be compared with the data from multiplier (MULTIPLY) by using eight bit comparator, COMPM8 and will produce SPWM pattern then connect to switch selector to ensure that the SPWM pulse follows the switching sequence as in Table 1.

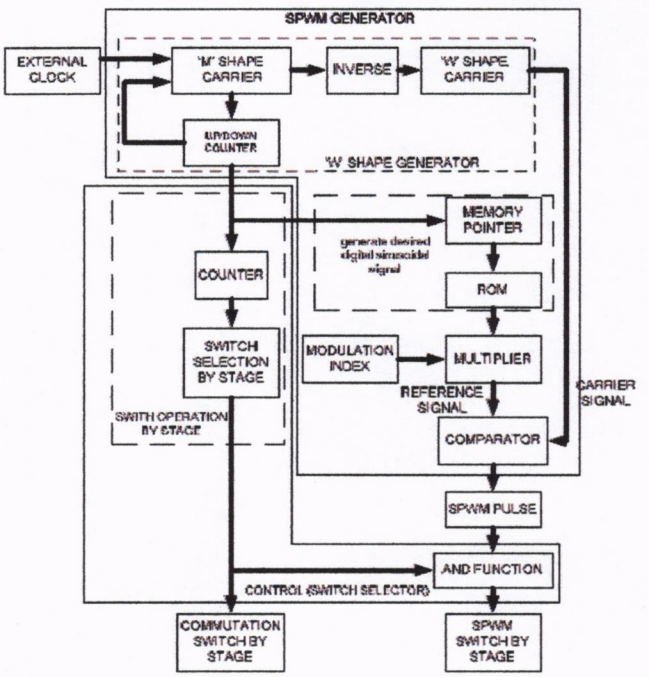


Figure 15 : FPGA SPWM Generation Algorithm for Inverter Operation

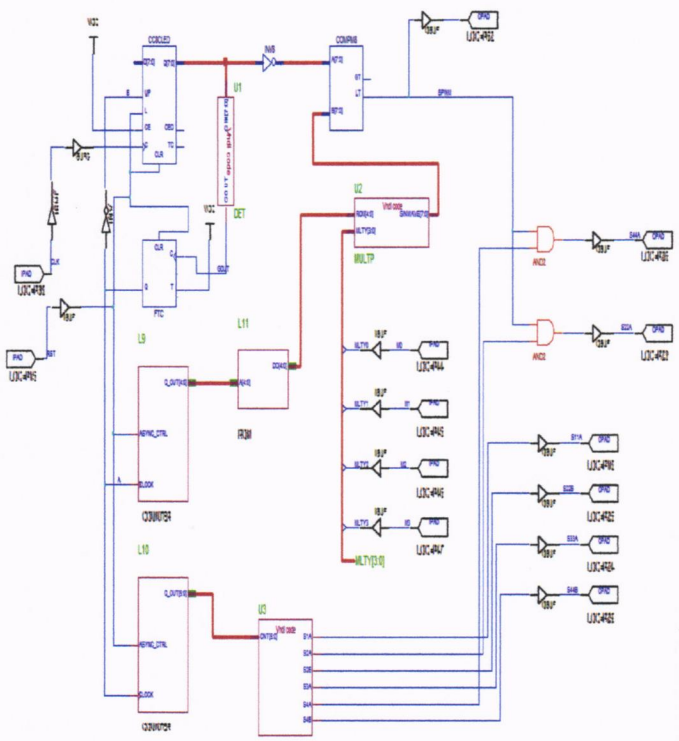


Figure 16: Schematic Diagram of XILINX FPGA

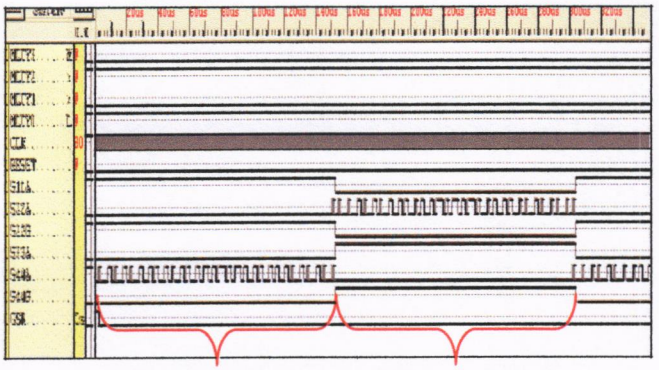


Figure 17: FPGA Simulation output

IX. HARDWARE IMPLEMENTATION

The inverter using Single Phase Matrix Converter (SPMC) was supplied by 20V DC and loaded with R=50Ω, L=4mH and C=10μF operated at modulation index, ma=0.5 with switching frequency, fs=5kHz. 5V DC supply is used to power the XILINX FPGA board and gate-drive circuit whilst 15V was supply to the power circuit. The block diagram for implementation is as shown in Fig.18 with the laboratory test-rig as shown in Fig. 19. With switching strategy that includes safe commutation strategy and the use of Sinusoidal Pulse Width Modulation (SPWM) as illustrated in Fig. 8. Switching combinations are compiled as shown in Table 1 with details of full switching implementation as in Figs. 5 and 6.

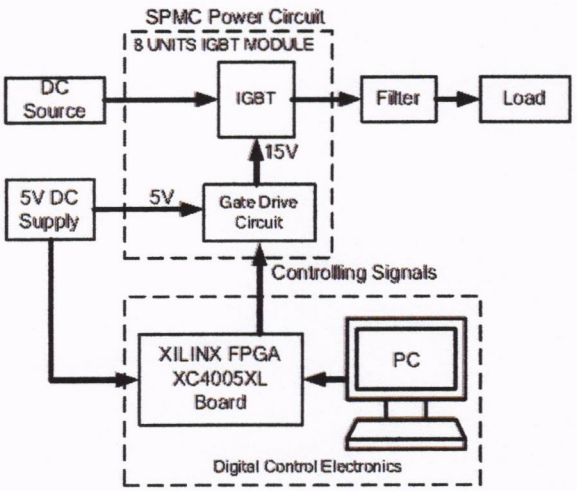


Figure 18 : The Experimental Set up

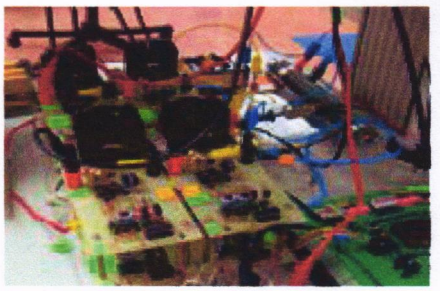
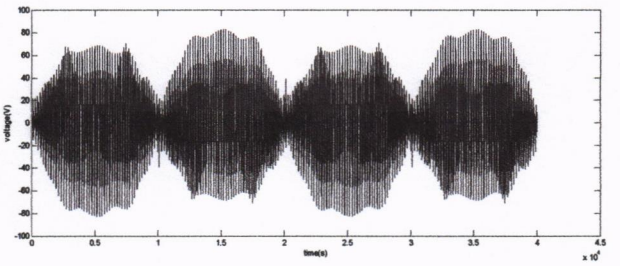


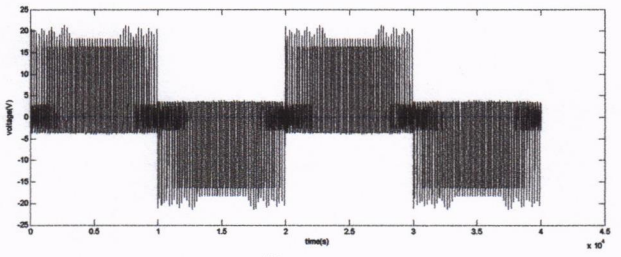
Figure 19 : Laboratory Test-Rig

X. RESULTS

Figure 20-27 represent the investigation on commutation strategy implementation when inductive and resistive loads are used. Fig. 20a and 21a are the sample obtained from simulation to illustrate the operation of inverter in producing the square form of the output voltage and output current without safe-commutation arrangement. Notice the spikes produced are of the order of 5 times (100V) the input value of 20V. Fig. 20b and 21b are the resulting waveform that is obtained with implementation of safe-commutation strategy as proposed. Fig. 24a, 24b, 25a and 25b is the result measured experimentally that indicating similar behaviour obtained. With the introduction of proper filter, we could actually produce a sinusoidal waveform as shown in Figure 22a, 22b, 23a and 23b, where Fig. 26a, 26b, 27a and 27b is the result measured experimentally that indicating similar behaviour obtained.

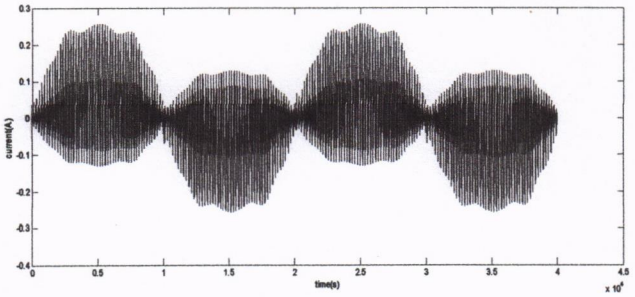


(a)



(b)

Fig. 20: Simulation result at voltage output across RL load
(a) without safe-commutation (b) with safe-commutation



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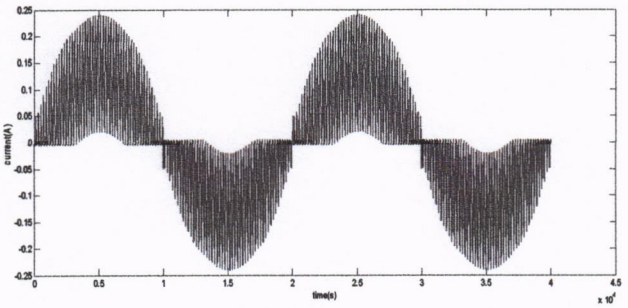
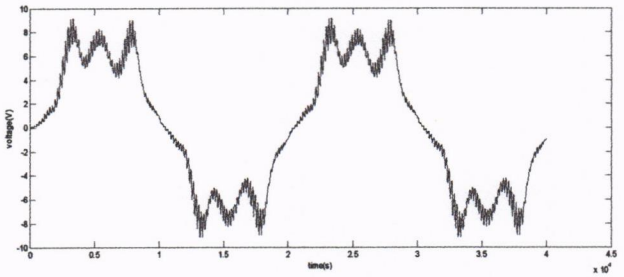
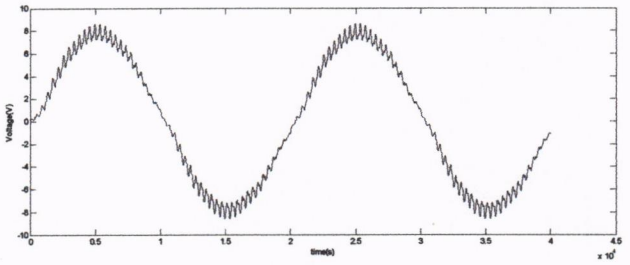


(b)

Fig. 21: Simulation result at current output at RL load
(a) without safe-commutation (b) with safe-commutation

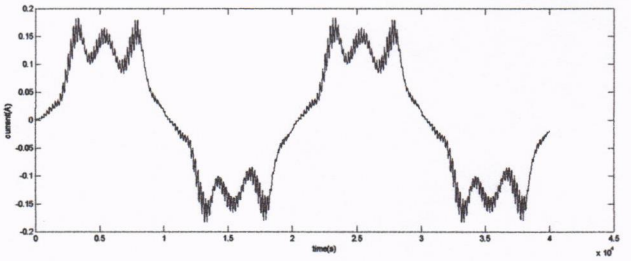


(a)



(b)

Fig. 22: Simulation result at voltage output across R load with LC filter
(b) without safe-commutation (b) with safe-commutation



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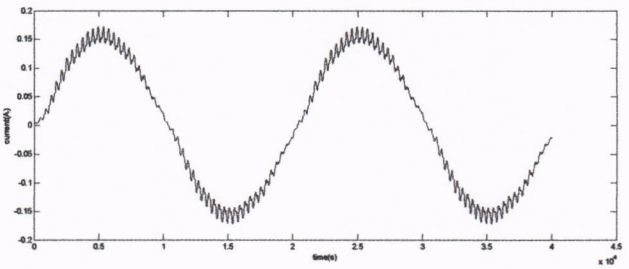
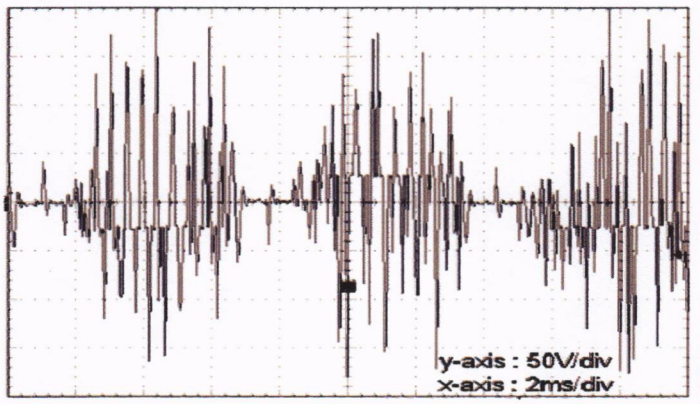


(b)

Fig. 23: Simulation result at current output at R load with LC filter
(a) without safe-commutation (b) with safe-commutation



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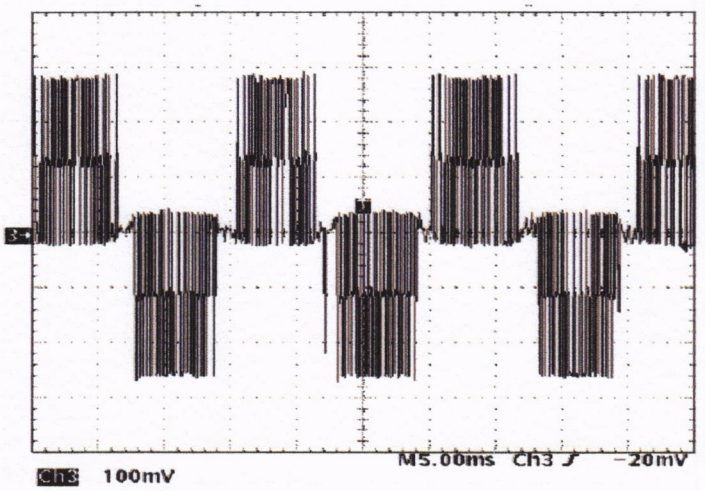
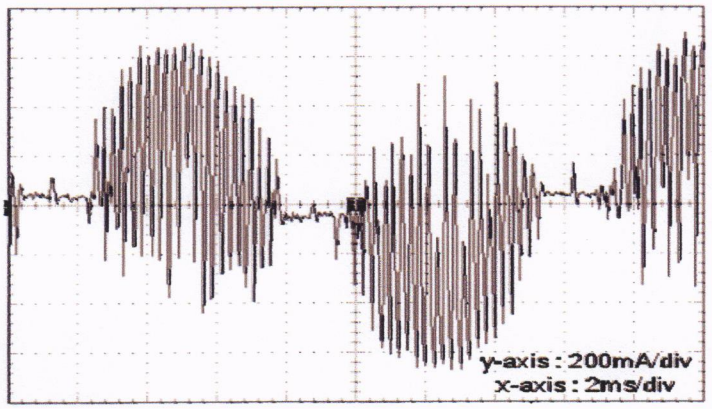
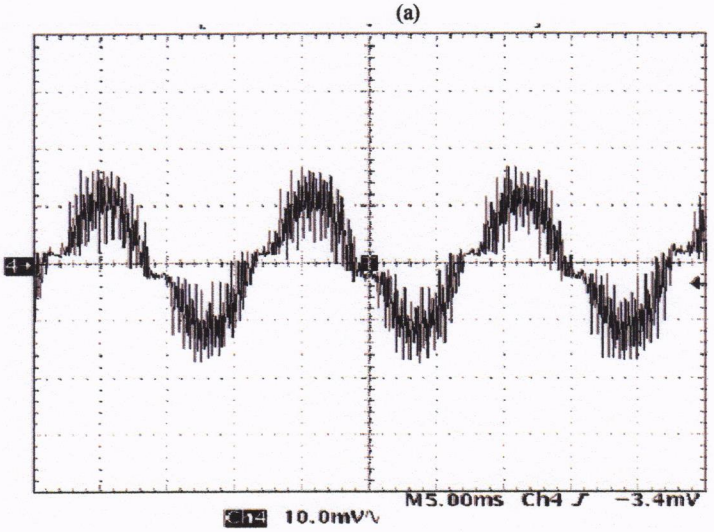


(b)

Fig. 24: Experimental result at voltage output across RL load
(a) without safe-commutation (b) with safe-commutation

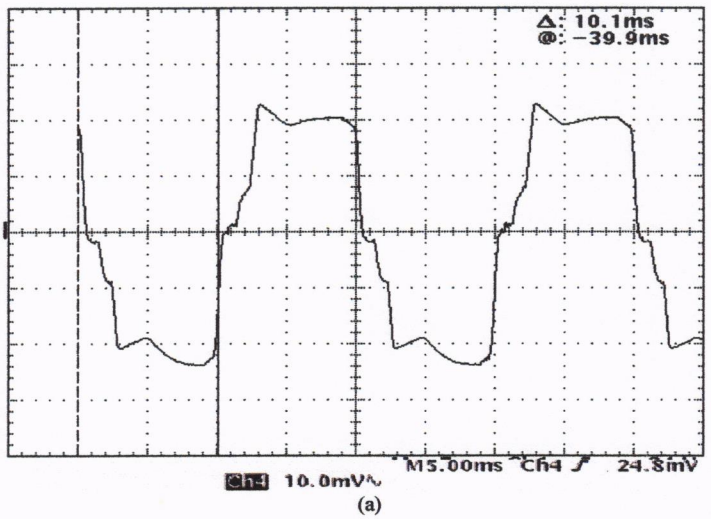


(a)

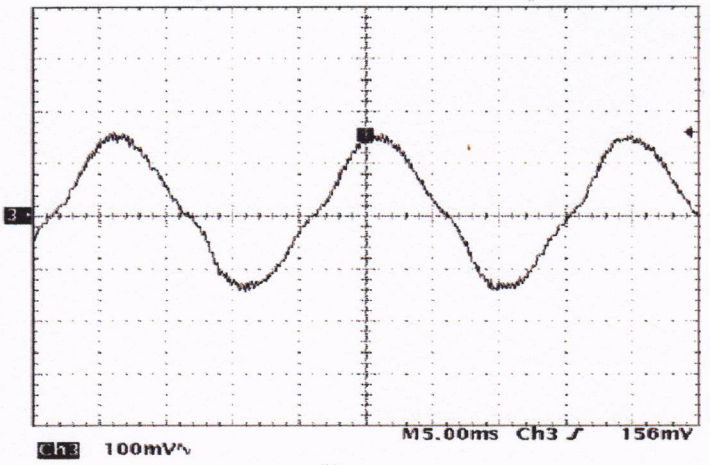


(b)

Fig. 25: Experimental result at current output across RL load
(a) without safe-commutation (b) with safe-commutation

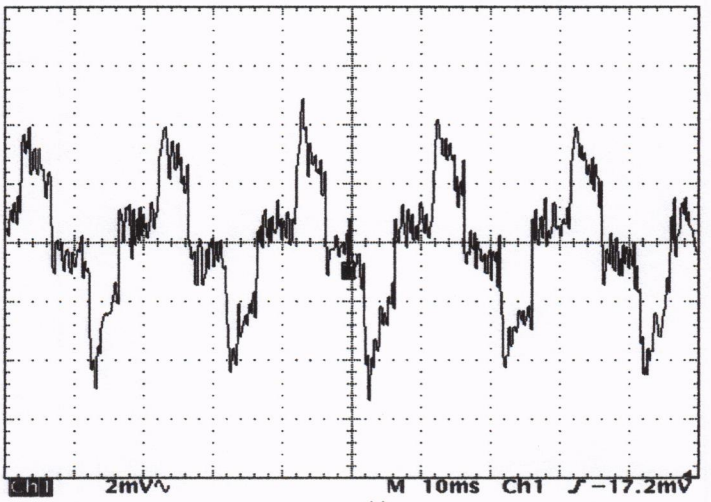


(a)

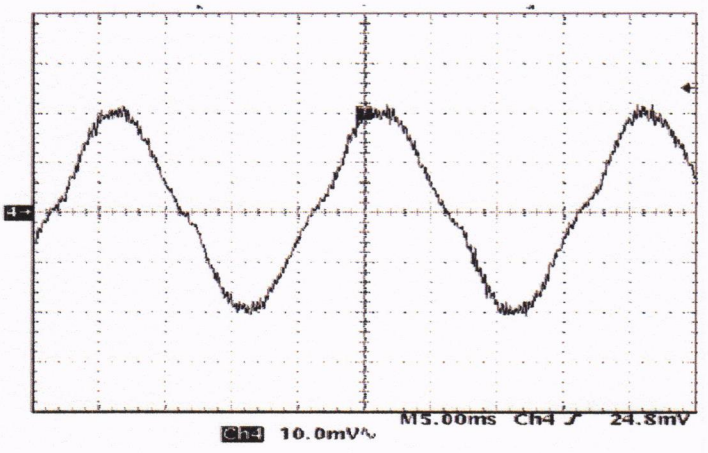


(b)

Fig. 26: Experimental result at voltage output across R load with LC filter
(a) without safe-commutation (b) with safe-commutation



(a)



(b)

Fig. 27: Experimental result at current output across R load with LC filter
(a) without safe-commutation (b) with safe-commutation

XI. CONCLUSION

This paper present safe commutation studies for switching strategy sequence of single-phase matrix converter (SPMC) as an inverter modulated by the Sinusoidal Pulse Width Modulation (SPWM) has been presented. The operational behaviour was verified using MATLAB/Simulink with the SimPowerSystem Block Set. The Insulated Gate Bipolar Transistor (IGBT) was used for the switching device. Results of the SPMC for both the simulation and experiments illustrates that similar results were obtained without any change. The safe-commutation technique implemented has resulted in a scheme that allows dead time to avoid current spikes of non-ideal switches and at the same time establishing a current path that could eliminate switching spikes due to the use of inductive load. As can be observed in the experimental results, good agreement was obtained with those predicted in simulations.

XII. FUTURE DEVELOPMENT

This project can be improved as listed below:

- Use the suitable capacitor that acts as a filter to reduce the ripple which produces from dc supply.
- Focus on Inverter operation in induction motor drive application for full investigations.
- This inverter operation can combined with rectifier operation in single circuit and become Uninterruptible Power Supply (UPS).
- Increase voltage to normal application level.
- Increase the switching frequency of operation to 20 kHz a normal application level associated with the limits of standard IGBT.
- PIC, Xilinx Spartan and Altera FPGA also can be used as digital electronic control implementation

XIII. REFERENCES

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