Characterization And Fabrication of 90nm PMOS with strained Silicon using TCAD Silvaco

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Abstract - **The paper is looking into the enhancement of conventional 90nm PMOS by using graded silicon germanium layer (SiGe) within the channel and bulk of semiconductor. The performance of conventional 90nm PMOS and 90nm PMOS with silicon germanium layer was compared. A process simulation of Strained Silicon PMOS and its electrical characterization was done using TCAD tool. The analysis focused on Id-Vg, Id-Vd characteristic, and hole mobility changes. The output characteristics were also obtained for Strain Silicon PMOS which showed an improvement of drain current compared with conventional PMOS.**

Keywords: **Strain silicon, SiGe, PMOS devices, Simulation**

1.0 INTRODUCTION

Rapid scaling of MOSFETs drives increasing microprocessors performance and rapid growth of the information technology revolution. The underlying principle behind the revolution is Moore's law. Moore pointed out that reduced cost per function is the driving force behind the exponential increase in transistor density. It is this exponential reduction in cost per function that drives microprocessor performance and growth of the information technology and semiconductor industry. Strained silicon is one of those rare new technologies that enables a fairly dramatic increase in performance with a relatively simple change in starting materials. Proof that transistors fabricate PMOS with strained silicon were faster due to increased electron mobility and velocity was first demonstrated in the mid-1980s. Then, in 1998, researchers showed it would work with leading-edge, sub-100 nm short-channel transistors. Today, companies such as Intel, IBM, Hitachi, AMD and UMC have reported success with strained silicon.

Strained silicon works by growing a thin layer of silicon on top of a layer of silicon germanium. There are two major types of induced strain that can be introduced in CMOS technologies for carrier mobility enhancement which are biaxial and uniaxial strain. Longitudinal tensile strain (strain along the channel, making it longer) allows holes to move more quickly and smoothly. In biaxial tensile strain, the interatomic distances in the silicon crystal are stretched, generally increasing the mobility of holes making p-type transistors faster [2].

The strained – Silicon is produces by depositing a thin layer of Silicon on an silicon germanium layer onto a Si substrate . The top Si layer is strained at the Si and SiGe interface because lattice of SiGe exerts a strain on the thinner top Si layer, stretching the Si layer slightly. Further, by controlling the amount of Ge in the bottom SiGe layer , the amount of strain produce in the overlying Si Layer can be manipulated.

The atoms in the silicon layer align with those in the slightly larger crystalline lattice of the SiGe (germanium atoms are larger than silicon). Figure 1.2 shows silicon germanium (SiGe) is placing under the silicon crystal. When the SiGe deposited to the silicon crystal, the structure of silicon crystal will strain due to wider distance of SiGe lattice.

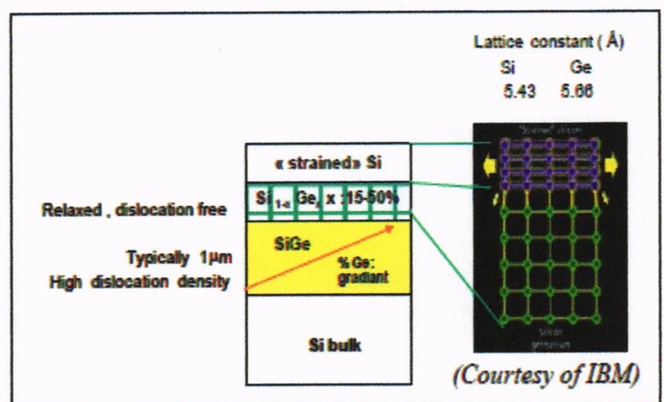

Figure 1. Straining silicon requires several epitaxial steps: a SiGe buffer on bulk Si; a relaxed SiGe template on the buffer SiGe; and Si on the relaxed SiGe template, which strains this top layer of silicon.

It was discovered that the lattice mismatch between Si and Ge atoms could be accommodated by a finite degree of lattice distortion. This distortion or strain actually offers the advantage of allowing electrons and holes to move faster. This increase in carrier mobility is attributed to a modified Si Band structure that lowers the resistance to electron and holes to movement in the material. The result is increased hole mobility in PMOS and electron mobility in NMOS devices. This leads to an increase in channel drive current and also some reductions in power consumption. [3].

This research is to study the effect of silicon germanium layer in the channel and show the enhancement in drive current due to incorporation of SiGe/Si heterostructure channel. Besides, this research also to investigate the effect of strained Si on hole mobility.

II. METHODOLOGY

Both strained silicon PMOS with an added SiGe layer and normal conventional PMOS device without SiGe layers process simulation were carried out using ATHENA, Figure 1 shows the structure of both devices. The simulation process to create the strain silicon PMOS is similar to the conventional PMOS fabrication process. The conventional 90nm PMOS process specification was referred as in Table 1.

Table 1: Process specification

No	Process	Material / Dose / Dimension
1	Initial substrate	Phosphorus 2e18 atom/cm^3
2	Well Oxidation	Dry O_2, diffuse time = 20 min, temperature = 900
3	Threshold Voltage Adjust	Boron 1.3e18 atom/cm^3
4	Gate Oxide Growth	36.7 A
5	Polysilicon Gate	90nm length gate
6	Spacer	Nitride 0.15 thick
7	Source Drain Implantation	boron 1e15 atom/cm^3 20 kev
8	Metallization	Aluminum 0.75µm thick

The fabrication process flow of the conventional 90nm PMOS device was simplified as follow. All this process was simulated in ATHENA:

- Initial substrate is p-type material
- Well oxidation
- Vt adjust implant
- Gate Oxide grow (36.7A)
- Polysilicon formation (Lg = 90nm)
- Spacer formation (Nitride thick = 0.15µm)
- Source Drain Implantation
- Metallization formation

The difference between the Strain Silicon PMOS structure with the conventional structure is that there is added SiGe layer. The Strain Silicon PMOS process specification was referred as in Table 2.

Table 2: Process specification

No	Process	Material / Dose / Dimension
1	Initial substrate	Phosphorus 2e18 atom/cm^3
2	Well Oxidation	Dry O_2, diffuse time = 20 min, temperature = 900
3	Threshold Voltage Adjust	Boron 1.3e18 atom/cm^3
4	SiGe and thick silicon deposition	Silicon 0.010µm thick Sige 0.015µm thick c.frac = 0.35 Silicon 0.007µm thick
5	Gate Oxide Growth	36.7 A
6	Polysilicon Gate	90nm length gate
7	Spacer	Nitride 0.15 thick
8	Source Drain Implantation	boron 1e15 atom/cm^3 20 kev
9	Metallization	Aluminum 0.75µm thick

The Strain Silicon PMOS structure is created with the thickness 0.010 µm is deposited on the silicon substrate. Then a silicon germanium (SiGe) layer with the thickness of 0.015 µm is deposited on the silicon layer, followed by deposition of another silicon layer with 0.007 µm thickness to the SiGe layer. After the deposition, strained silicon is created at the channel. The flow chart process of 90nm PMOS with graded SiGe summarized as Figure 2. In Strained Silicon PMOS, the fraction concentration for gemanium content in SiGe chosen to be 0.35 meanings that 35% of SiGe consist of germanium material and the dopant impurity of boron to 3e15 atom/cm3. This syntax was included in Athena input file:

"deposit silicon thick=0.010 divis=4 c.phos=1e16"
"deposit sige thick=0.015 divis=5 c.frac=0.35 c.phos=1e16"
"deposit silicon thick=0.007 divis=4 c.phos=1e16"

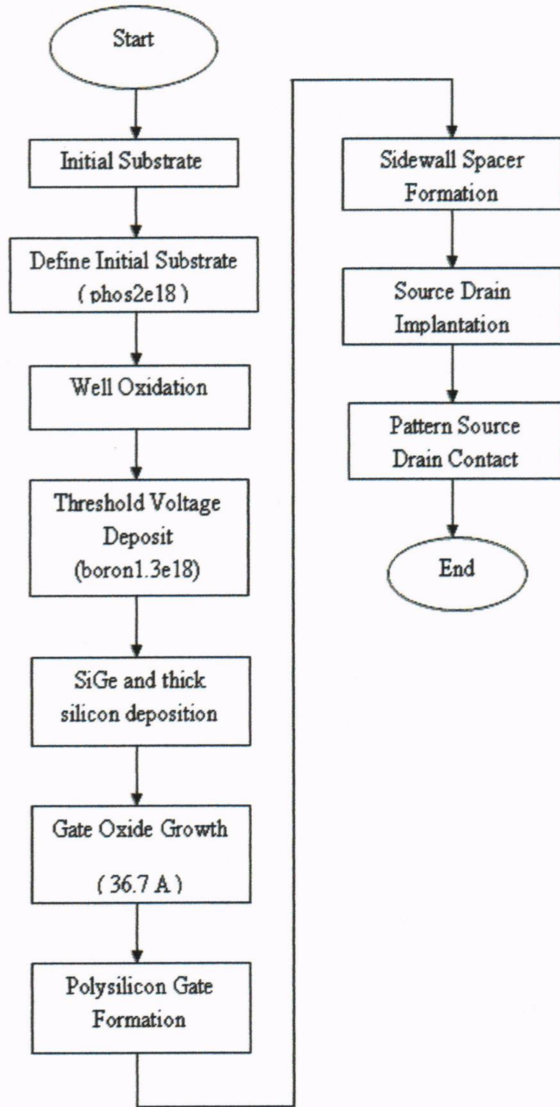

Figure 2: Flow chart of PMOS with SiGe

Finally, the final structure of the conventional 90nm PMOS and PMOS with SiGe was shown in figure 3(a) and figure 3(b).

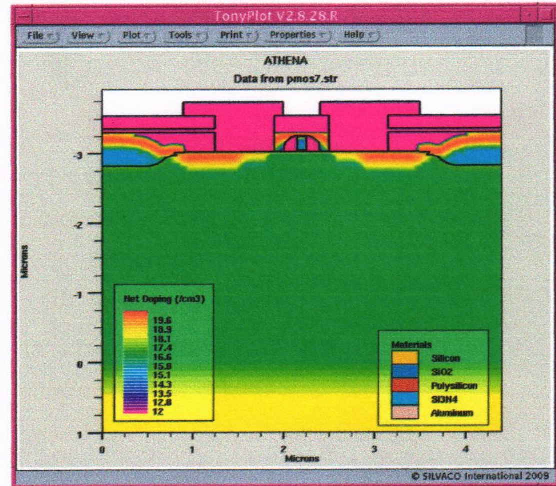

Figure 3 (a) Conventional 90nm PMOS

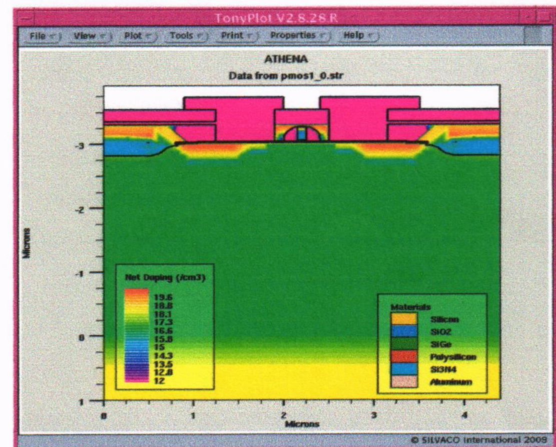

Figure 3 (b) 90nm SiGe

ATLAS was used as device simulator to measure electrical characteristic of each device. In order to find Id-Vg characteristics, Vg was varying from 0V to -1.2V with constant value of Vd that is 100mV.For Id-Vd characteristics, both structures are simulated to ramp the drain voltage, Vds to 100mV when the gate voltage, Vgs is bias to -0.5V, -0.8V and -1.1V V. These two devices tested with the same condition to observe electrical characteristic and differentiate between PMOS SiGe and without SiGe. Then the carrier mobility between PMOS conventional and PMOS using SiGe is compare by using equation below. Hole mobility was calculated based on equation below using saturation current Id_{sat} in Id-Vd curve.

equation (1):

$$\mathbf{Id_{sat}} = \frac{\mu\, Cox\, W}{2L}(\mathbf{Vgs} - \mathbf{Vt})^2$$

μ = mobility hole

III. RESULTS AND DISCUSSION

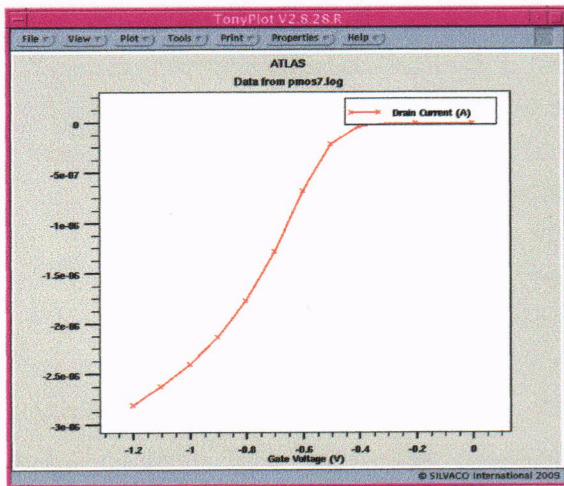

Figure 3 : Id-Vg curve for Conventional 90nm PMOS

From the simulation, the drain current, Id versus gate voltage, Vgs curve with a drain voltage, Vds of 100mV for conventional PMOS. The measured threshold voltage was -0.437378V with optimized Vt adjust of 1.0e18 atoms/cm3 Boron material as illustrated in Figure 3. Ion was measured to be -2.80368e-06A/um while Ioff -3.37684e-12 A/um.

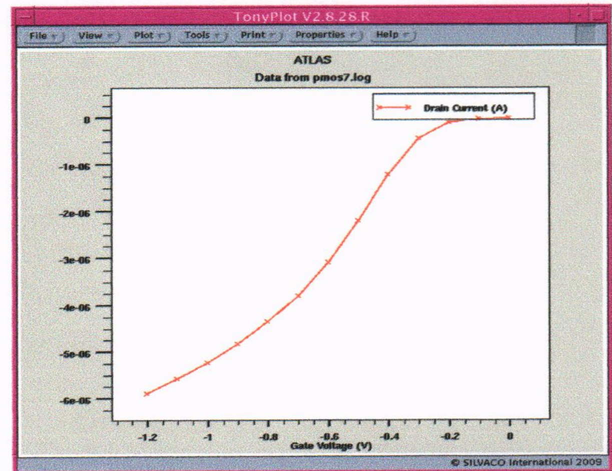

Figure 4 : Id-Vg curve for 90nm PMOS SiGe

From the Figure 4, Vth for PMOS using SiGe was reported to be -0.228035V with Ion and Ioff equal to -5.87929e-06 A/um and -1.57952e-09 A/um respectively. The measurement shows that PMOS SiGe provide higher Idmax (Ion) compared to conventional PMOS and higher current leakage (Ioff) during the same test. From the result show that the drain current for Strain Silicon PMOS structure is higher than conventional PMOS. This indicates that the Strain Silicon PMOS has higher drive current compared to conventional PMOS. Meanwhile the extracted threshold voltage are -0.228035V and -0.437378V for the Strain Silicon PMOS and conventional PMOS respectively. This indicates that the strained PMOS has lower voltage threshold than the conventional PMOS which translates to lower power consumption. This result shows that the silicon under the gate experience compressive stress during ion implantation process source and drain. Essentially SiGe layer will relax the thin silicon as shown in figure 1 which compressive stress was expected to induce by dopant concentration during ion implantation process. Since the thick silicon under the gate experience compressive stress cause the inter-atomic distances are shortened and it allow heavy hole to move easily through the structure . This will increase the mobility of hole and drain current and thus improving transistor switching speed. Differently with NMOS that consist of electron as majority carrier that can increase the drain current when experience tensile strain because the inter-atomic distances of this structure are larger and allow light electron to move faster and improve the performance of NMOS.

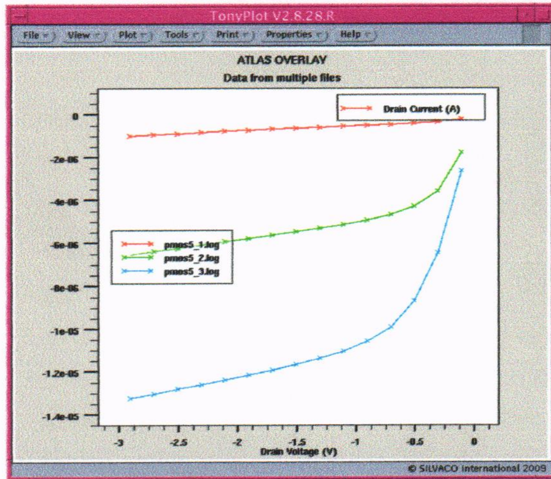

Figure 5: Id-Vd curve for Conventional 90nm PMOS

Beside that, conventional PMOS structures was simulated to ramp the drain voltage, Vds to 100mV when the gate voltage, Vgs is bias to -0.5V, -0.8V and -1.1 V. The simulation results are presented in Figure 5 which represents the graph of the drain current versus the drain voltage. From The simulation, with the test voltage at Vg=-1.1V resulted Idmax to be -1.32052e-05 A/um

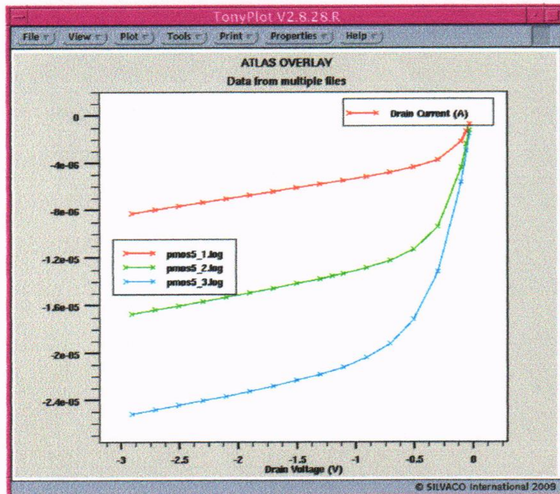

Figure 6: Id-Vd curve for 90nm PMOS SiGe

Since Id-Vg curve show the increase of Idmax, same goes to the Id-Vd for the same gate voltage using SiGe as illustrated in Figure 6. This proven with the test voltage at Vg=-1.1V resulted Idmax to be -2.50815e-05 A/um. From Figure 6, it can be seen that the strained PMOS device has a higher drive current compared to the conventional PMOS. From these results, it is evident that the strained silicon PMOS has a better drive current than conventional PMOS.

Table 3 : Comparison result between conventional 90nm PMOS and PMOS with silicon germanium (SiGe)

Parameters		Conventional 90nm PMOS	90nm PMOS SiGe
Vth		-0.437378V	-0.228035V
Ioff (A/um)		-3.37684e-12	-1.57952e-09
Ion (A/um)		-2.80368e-06	-5.87929e-06
Idsat	Vg=-1.1V	-1.32052e-05	-2.50815e-05

IV. CONCLUSION

In conclusion, after simulated 90nm conventional PMOS and PMOS with SiGe, it can be seen that the Strain Silicon PMOS has a better performance compared to conventional PMOS. This can be shown from the comparison result between both structure in electrical characteristic of each Id-Vg and Id-Vd.The result show that the significant increase of hole mobility and drain current compared to conventional PMOS. It shows that 90nm PMOS using graded silicon germanium on the channel is suitable to improve the performance of PMOS.

V. FUTURE DEVELOPMENT

In order to improve performance of PMOS, this research will continue to study the electrical characteristics of the strain Silicon PMOS such as the effective mobility enhancement. . Strained silicon is still considered as a new technology and more research is still needed to improve its implementation to the current technology like other technology, the use of SiGe in the source and drain to induce compressive stress in the PMOS channel region.

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