POWER EFFICIENT 64-BIT DYNAMIC COMPARATOR USING 0.18µm TECHNOLOGY

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Abstract— **This paper presents the comparative study on 64-bit dynamic comparator using different technology. The objective of the paper is to study and compare the speed of the comparator and to compare the power consumption for comparator in 0.5µm and 0.18µm technology. Comparator is a device that compares two inputs and chooses the high/low or same value to be the output. The tools used in designing comparator are SILVACO GATEWAY for schematic design. Result show that the power consumption is and the delay is 3.81nW and the delay is 142.98ps.**

Keywords- dynamic CMOS; equality comparator.

I. INTRODUCTION

Comparator is a special combinational circuit use to compare two inputs/magnitude and the output are A=B, A<B or A>B [1]. The comparator chose the high value or low value as the output depends on the inverting or non-inverting inputs that trigger the output to be chosen according to the circuit needed. Comparator is the simplest circuit use to convert analog or digital to create relevant outputs [2]. Several parameters needed to be considered when designing the comparator such as width and length of the transistor; the speed, power consumption and chip area are the important factors while designing comparators [2]. Technology chose also one of the factors that affect the delay and power consumption of the comparator. Comparators are used in central processing units (CPUs) and microcontrollers (MCUs). High-speed operation has always been a target in circuit design because of the speed demand for technology today [3]. A critical operation in comparator is the comparison of two binary input data. Theoretically, the fastest comparator is made of full combinational logic gates. NMOS and PMOS transistors of static CMOS gate are dual of each other; one of them will always be arranged in series. These transistors will increase the loading seen by the previous stages.

II. DYNAMIC COMPARATOR

A. Equality Comparator

An equality comparator is not a magnitude comparator. It has an output only show A = B. Example of inputs and output shown in Table I and Table II. When A = 1 and B = 1, output will be set active showing that A = B. Same case also applied when input A = 0 and B = 0 but when input A = 0 and input B = 1 or vice versa, output will show 0 showing that A not equal to B. Example of equality comparator can be shown in Figure 1. The propose design equality comparator shown in Figure 2[4].

TABLE I. TRUTH TABLE 2 INPUT EQUALITY COMPARATOR

INPUT		OUTPUT
A	**B**	**A = B**
0	0	1
0	1	0
1	0	0
1	1	1

TABLE II. TRUTH TABLE 4 INPUT EQUALTY COMPARATOR

INPUT				OUTPUT
A_1	**A_0**	**B_1**	**B_0**	**A = B**
0	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	0	1	1	0
0	1	0	0	0
0	1	0	1	1
0	1	1	0	0
0	1	1	1	0
1	0	0	0	0
1	0	0	1	0
1	0	1	0	1
1	0	1	1	0
1	1	0	0	0
1	1	0	1	0
1	1	1	0	0
1	1	1	1	1

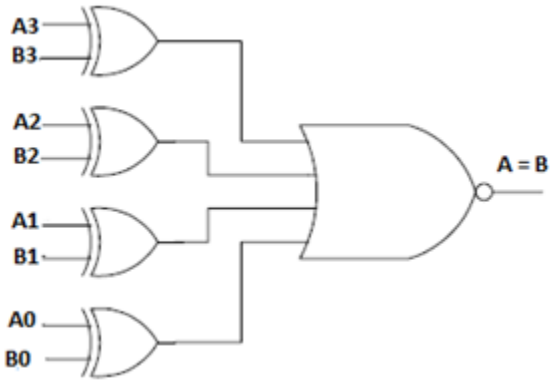

Figure 1. Equality comparator

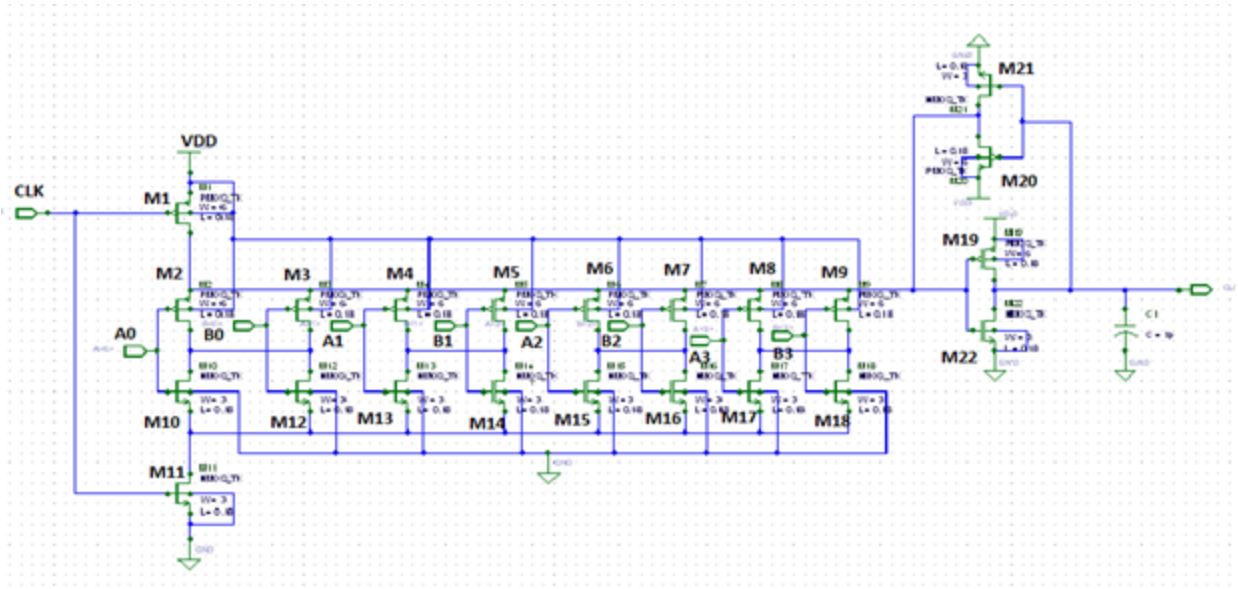

Figure 2. Proposed equality comparator design

B. *Zero/one comparator*

The same design methodology can be implemented to the zero/one detector. Large fan-in AND or OR gates requires to detect all zeros and all one. This problem can be overcome by designing a tree of AND gates as shown in Figure 3[5]. The proposed circuit of an 8-bit zero/one comparator is shown in Figure 4[4]. When the CLK is low, Node 0 is precharged to VDD. When REF is set high, D0, D1, D2, D3, D4, D5, D6 and D7 also high, then M15, M16, M17, M18, M19, M20, M21, M22, M23 and M24 are on while M2, M3, M4, M5, M6, M7, M8, M9 and M10 are all off. So, Node 0 kept in high and there is no current path exists during the period [4].

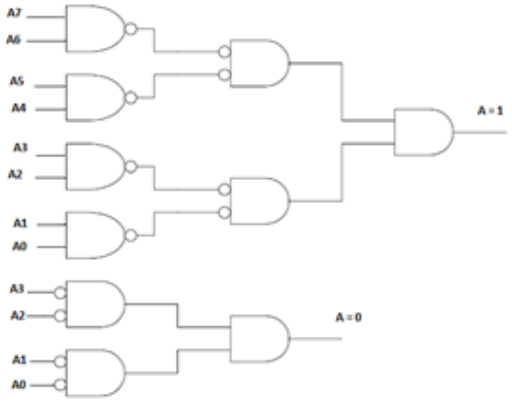

Figure 3. Tree of AND gates

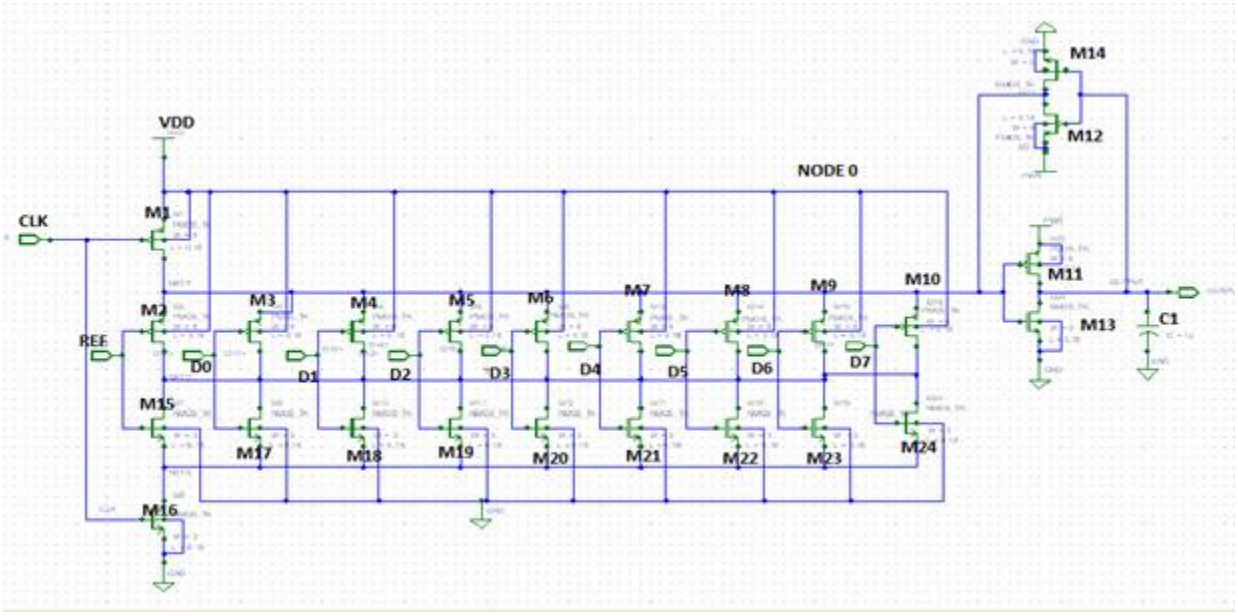

Figure 4. Proposed zero / one circuit

C. Inverter

At the end of the equality circuit, there are two inverters. The inverters are used at the output as a buffer to prevent drawback output. Figure 5 show the inverter using NMOS and PMOS. Inverter output tested in the SILVACO before generating the symbol. When input A = 1, output Y = 0 and vice versa. Buffer also use to amplify signal and to increase gate's current capability [6].

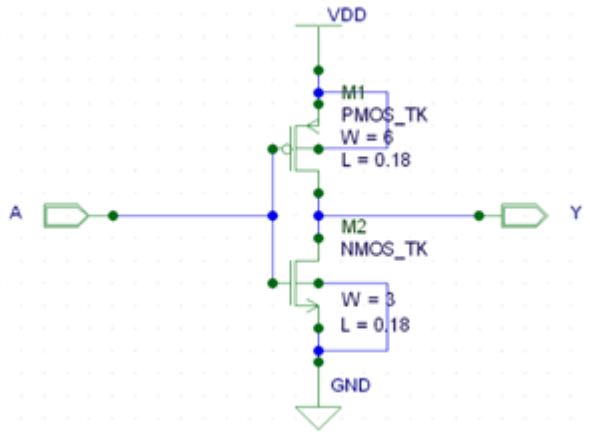

Figure 5. Inverter

III. DESIGN OF THE COMPARATOR

The flow chart on Figure 6 shows the step to design the power efficient 64-bit dynamic comparator using 0.18µm technology. Same steps taken to design the 0.5µm technology comparator and the result are compared with 0.18µm technology.

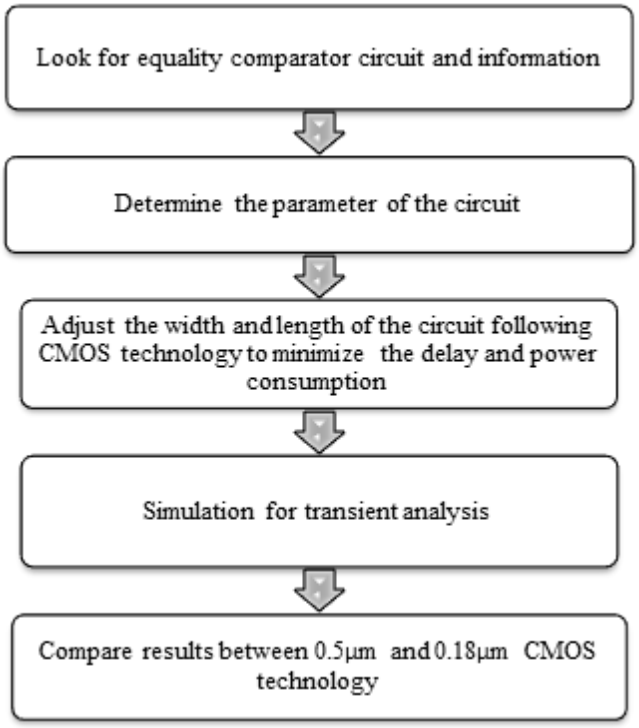

Figure 6. Flowchart of the project

The parameters of all the transistors are shows in Table III. These MOS parameters are for 0.18µm technology.

TABLE III. MOS PARAMETERS

	All PMOS	*All NMOS*
Width	6µm	3µm
Length	0.18µm	0.18µm

IV. SIMULATION RESULTS AND DISCUSSION

Simulation for transient analysis is done using 0.18µm CMOS technology. 5V voltage supply is used and clock period used is 8ns for transient analysis. This design used to determine the power and delay/speed. Simulation results of the comparator are shows in Figure 7, Figure 8 and Figure 9. The width of the transistor used is as in the Table III. This simulation result is compared to the previous work by [4].

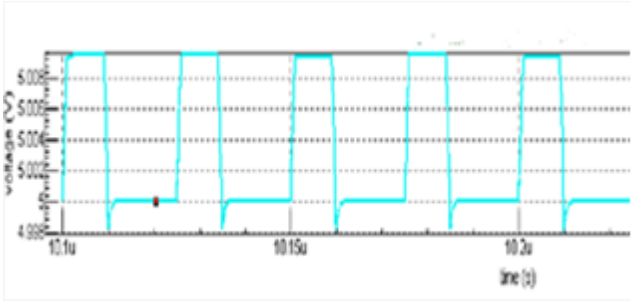

Figure 7. Output voltage waveform for 0.18µm technology

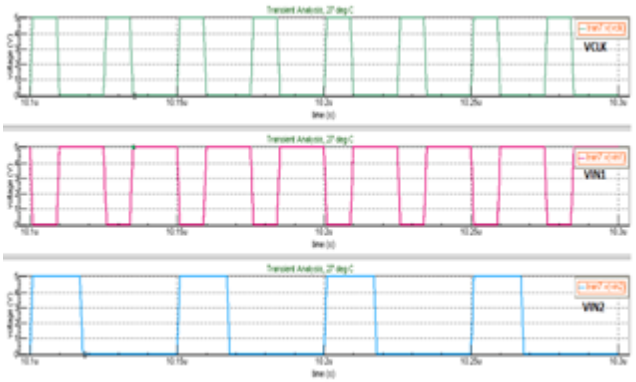

Figure 8. Input waveform for 0.18µm technology

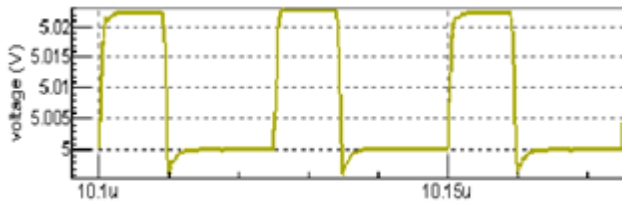

Figure 9. Output voltage waveform for 0.5µm technology

A. *Effect of parameter chosen*

0.18µm technology use in this project which is smaller length than technology used in the previous work by, so length of PMOS and NMOS for this project is 0.18µm. Simulation in Figure 10 shows the different in the output when different technology is chosen.

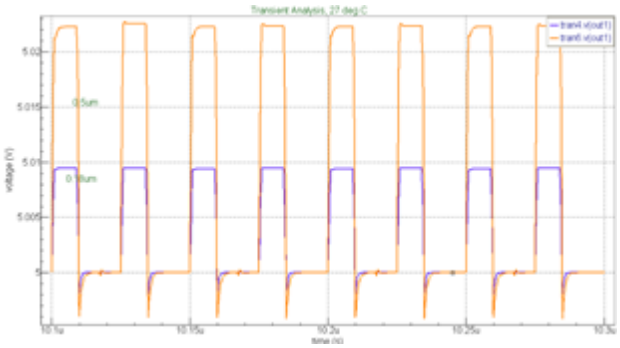

Figure 10. Output waveform with different length

B. *Propagation delay of the comparator*

Propagation delay and settling time are the most important parameters to determine the speed of the comparator designed. Propagation delay is the amount of time that it takes for a change in the input signal to produce a change in the output signal. Delay time is measured at 50% transition of the point. The propagation delay is determined using two basic time intervals, which is t_{PLH} and t_{PHL}. t_{PLH} is the delay time measured when output is changing from logic 0 to logic 1 and t_{PHL} is from logic 1 to 0[7]. Propagation delay is the sum of t_{PLH} and t_{PHL} and then divides by 2. In this project, delay is measured using the SILVACO tools. Different technology produces different delay. The smallest delay, the fastest the speed. Figure 11 and 12 show the different delays when using different CMOS technology.

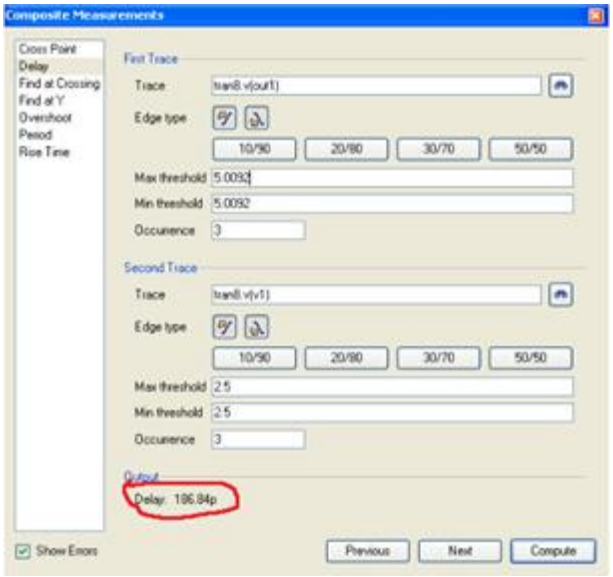

Figure 11. Delay 0.5µm technology

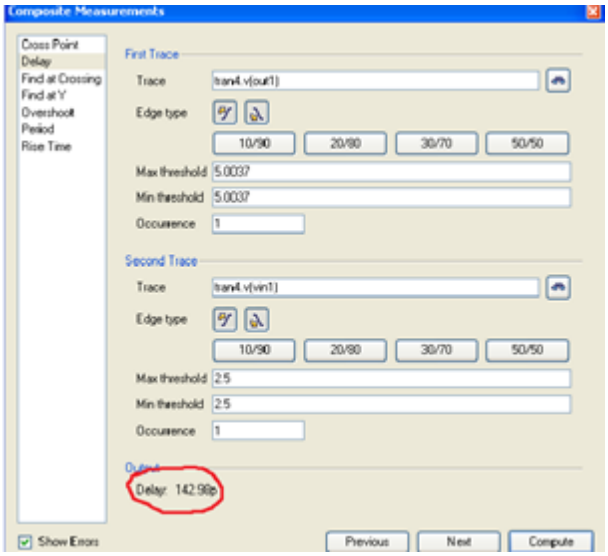

Figure 12. Delay 0.18µm technology

Simulation shows that the delay of 0.18µm technology (142.98p) is smaller than the 0.5µm technology (186.84p). This shows that the 0.18µm technology is faster than 0.5µm technology. The speed of the comparator has increase 93% than the previous technology [4].

C. Power dissipation

Next important parameter is the power dissipation of the comparator [8]. Power dissipation need to be reduced to reduce noise and cost. Power dissipation is power that is transform into a heat and then radiated away from thedevices. Power dissipation can be determined by multiply the current, I_{DD} with the supply power, V_{DD} as shown in Eq. (1)[9].

$$P = V_{DD} \times I_{DD} \quad (1)$$

Figure 13 shows the total current of the 0. 5µm technology and Figure 14 shows the total current of the present work using 0.18µm technology. From Eq. (1) [4], the power dissipation for 0.5µm technology is 3.67nW and for the current work is 3.81nW. The power dissipation for 0.18µm technology is higher than 0.5µm technology. Although the power is high, the power range is still 3.5nW – 4.0nW. So, this comparator is still power efficient although it using smaller technology. Theoretically, when the speed is increase, the power also increases.

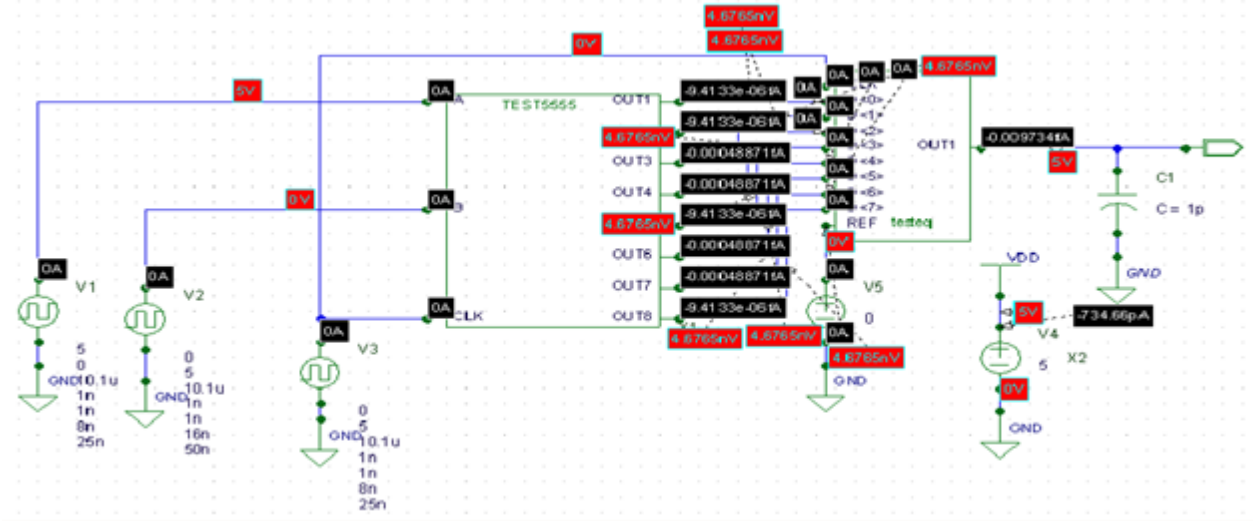

Figure 13. Total current for 0.5µm technology

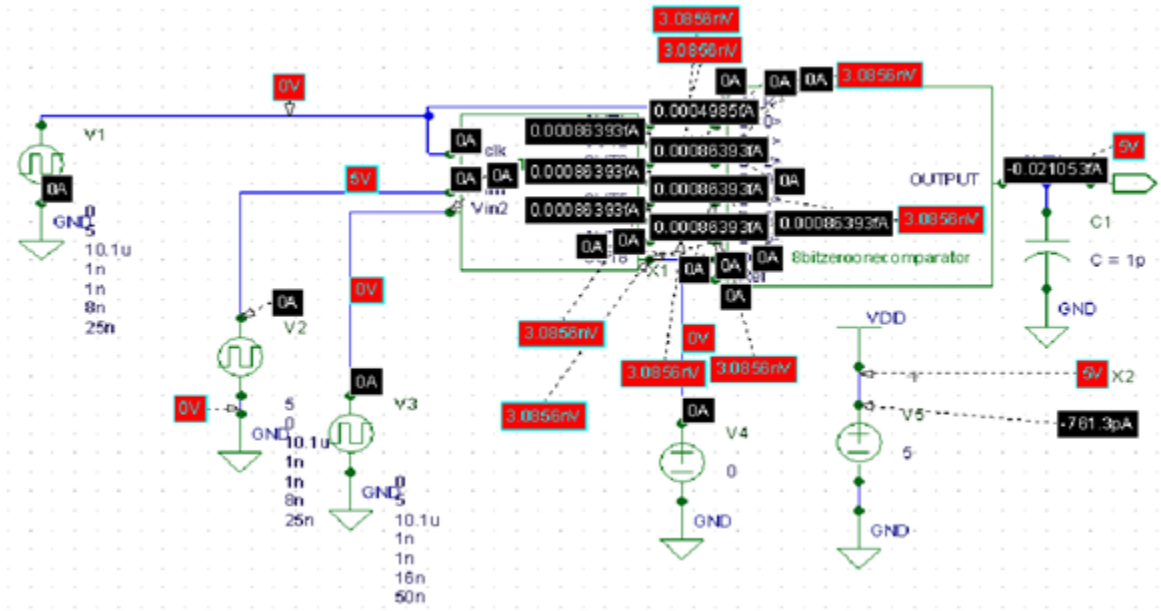

Figure 14. Total current for 0.18µm technology

D. Average dynamic power dissipation

Average power is the energy converted per unit of time. The energy consumed over some interval time, T is the integral of the instantaneous power [8].

$$E = \int_0^T I_{DD}(t)V_{DD}dt \qquad (2)$$

The average dynamic power dissipation over this interval is shows in Eq. (3) [8].

$$P_{avg} = \frac{E}{T} = \frac{1}{T}\int_0^T I_{DD}(t)V_{DD}\,dt \qquad (3)$$

The integral finds the average current delivered by VDD. Using the SEedit, average dynamic power can be measured automatically. Results of the average dynamic power dissipation are shown in Figure 15 and 16.

Index	tran6.p(v4)[W]
1	3.67328e-009

Figure 15. Measured power of 0.5µm technology

Index	tran4.p(v5)[W]
1	3.80648e-009

Figure 16. Measured power of 0.18µm technology

V. CONCLUSION

This paper has presented the power efficient dynamic comparator using 0.18µm technology. Author has compared the results with the previous work that using 0.5µm technology for the simulation as comparison using 5V power supply [4]. Table IV show the comparison between 0.5µm and 0.18µm technology. 5V voltage supply was used for both technologies but the CMOS technology is different. This project wants to determine of the effects when different CMOS technology used in a comparator without disturbing the value of voltage supply.

The smaller technology use, the faster the comparator speed but it increases the power dissipation of the comparator.This project can be improved by using a smaller CMOS such as 65nm.

TABLE IV. COMPARISON OF THE PRESENT COMPARATOR DESIGN WITH THE 0.5UM TECHNOLOGY

	0.5µm	**0.18µm**
Length	0.5µm	0.18µm
Wp/ Wn	10µm/5µm	6µm/3µm
Voltage supply	5V	5V
Delay	186.84ps	142.98ps
Power dissipation	3.67nW	3.81nW

ACKNOWLEDGMENT

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