Detection of Faulty Pilot Cable Using ALTERA Cyclone II Board with Time-Domain Reflection (TDR) Technique

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***Abstract*- This project implements digital technique to control the inspection wires in pilot cable by using ALTERA Cyclone II board. It is the advancement of time-domain reflection (TDR) technique for faulty cable detection. The TDR module generates pulse signal and it will be injected into the inspection wire. The edge and reflection signal from the inspection pilot cable are recorded by the digital sampling oscilloscope (DSO). By analyzing the shape of reflected pulse signal (in step waveform) using oscilloscope, the type and location of fault cable can be determined. This entire module is coded using Very High Speed Integrated Circuit Hardware Description Language (VHDL).**

***Index Tern*-Time-Domain Reflection (TDR), Digital Sampling Oscilloscope (DSO), Very High Speed Integrated Circuit Hardware Description Language (VHDL).**

I. INTRODUCTION

The pilot cable is normally used for control signaling, telecommunication, protection and data transmission purposed associated with power distributed and transmission system. Pilot cable is complying with the customer requirement of Tenaga National Berhad (Malaysia Utility Company). Pilot channel provide channel between electricity supply substation for communication and for protective relaying of high voltage overhead and undergoes lines [3].

In the pilot cable there are bundle of wire enclosed in wire amour or single core round hard drawn aluminum wire applied helically (spiral-shaped) over them and covered by dual insulation with an inner core of cellular polyethylene and outer skin of solid polyethylene. An over voltage in pilot cable cores may compromise alarm system, resulting the severe damage to the power system and prevent equipment. However, the problems will occurs when the pilot cable along with transmission line enters swampy areas as water might seep into in and cause damage to it. Also there are others problems such as broken conductor, water damage, crimps and variety of other fault condition [2].

Thus, an efficient testing system such as TDR is used to monitor the cables. However, such system is fully in analogue which is not only bulky but it also needs more power to operate the system. The pulse to be sent to the cable is about 9V and it can be reduced to smaller power if the system is developed using CMOS technology.

This paper proposes new technique to replace the analogue TDR. The proposed model for new TDR is developed using VHDL and it is implemented on ALTERA Cyclone II Board. The experimental results also verify the model is capable to detect faulty cable.

II. OPERATION OF TDR SYSTEM

The method of controlling the signal pulse generated by ALTERA Cyclone II board on TDR technique designed to detect damage pilot cable. The demultiplexer is able to monitor the waveform signal from which the wire being tester according to the input that the user design. The waveform signal appear on the oscilloscope is resulting of reflection waveform when the signal arrived at one end of the cable and travel back to the TDR. As the result, the output signal or reflected waveform on oscilloscope can be analyzed and determine the type of fault and the location of the fault on the pilot cable. Fig. 1 shows the operation block diagram of TDR module to detect faulty cable.

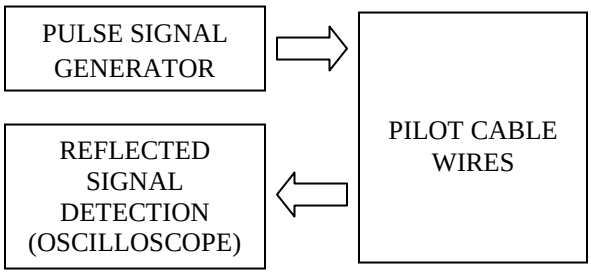

Fig. 1. Operation Block Diagram of TDR

The aim of this project is to improve the way to testing the pilot cable using TDR technique using digital system. This multiple output is able to send pulse signal to multiple pilot cable wires. There are 3 main modules for this design which are Pulse Generator, One to Sixteen Demultiplexer (demux) and Decade Counter. The design of these modules is using VHDL language than implement it into ALTERA Cyclone II board. Fig. 2 shows the design for this project.

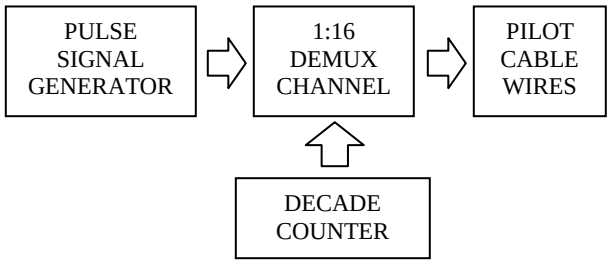

Fig. 2. Design of Block Diagram Module for This Project

The function of each module:

i. Pulse Generator – To generate pulse with repetition rate (frequency), pulse width and delay between pulses.

ii. Demultiplexer 1:16 Channel – To give the specific data from pulse generator to the cable. Data output to the cable is the same value as the data input.

iii. Decade Counter – to give specific data for selector of demux for counter propose.

A. Pulse Generator

Pulse generators usually allow control of the pulse repetition rate (frequency), pulse width, delay with respect to an internal or external trigger and the high- and low-voltage levels of the pulses [1]. For this project, the pulse that been use is 160ns with 2400ns delay between pulses. Fig. 3 shows the simulation of pulse generator that is been design.

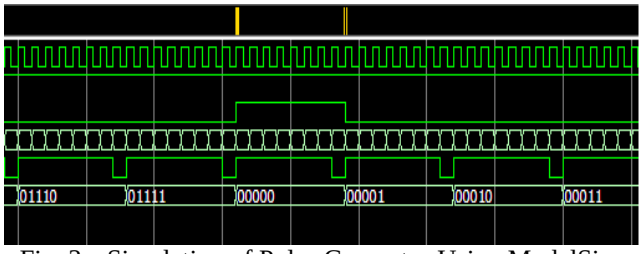

Fig. 3a. Simulation of Pulse Generator Using ModelSim

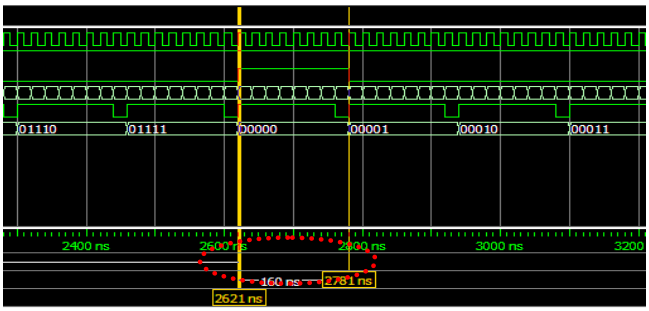

Fig. 3b. Pulse Generator with 160ns Pulse Width.

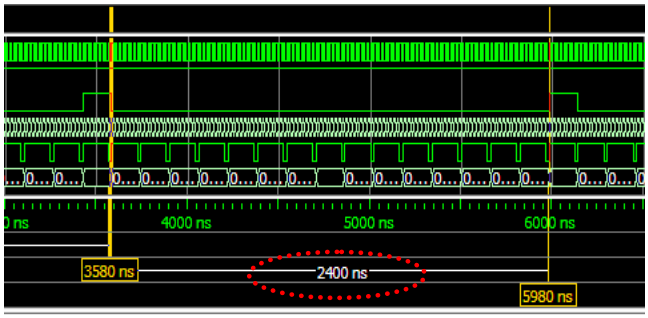

Fig. 3c. Pulse Generator with 2400ns Delay between Pulses

The basic concept to design the pulse generator by using VHDL code is the counter. Fig. 5 shows the flowchart of the pulse generator. The ALTERA Cyclone II board includes two oscillators that produce 28.86M hz and 50M hz clock signals. For this project, 50M hz clock is used for refection propose.

Process divider is used to count the width of the pulse. It had been set to "0000000000000111" for produced pulse width 160 ns. From 50M hz clock, the time clock is 20ns.

$$t = \frac{1}{f} = \frac{1}{50M} = \mathbf{20ns}$$

The process divider is sensitive to the 20ns clock and start counts from "0000000000000000" to "0000000000000111". The counts for divider are 8 of 20ns time clock that will produce 160ns pulse width.

$$\text{Pulse Generator Width} = 20\text{ns x } 8 = \mathbf{160ns}$$

For process count, it is designed for delay between pulses. Since the pulse width is 160ns, it is used for delay propose. Process count is counts from "00001" to "01111" which number of counts are 15.

$$\text{Delay Between Pulses} = 160\text{ns x } 15 = \mathbf{2400ns}$$

Fig. 4 shows the simulation result of pulse generator width and count made for delay between pulses.

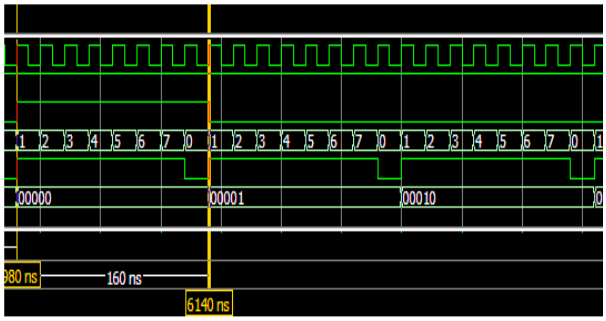

Fig. 4. Simulation of Pulse Generator Width and Count Made for Delay between Pulses

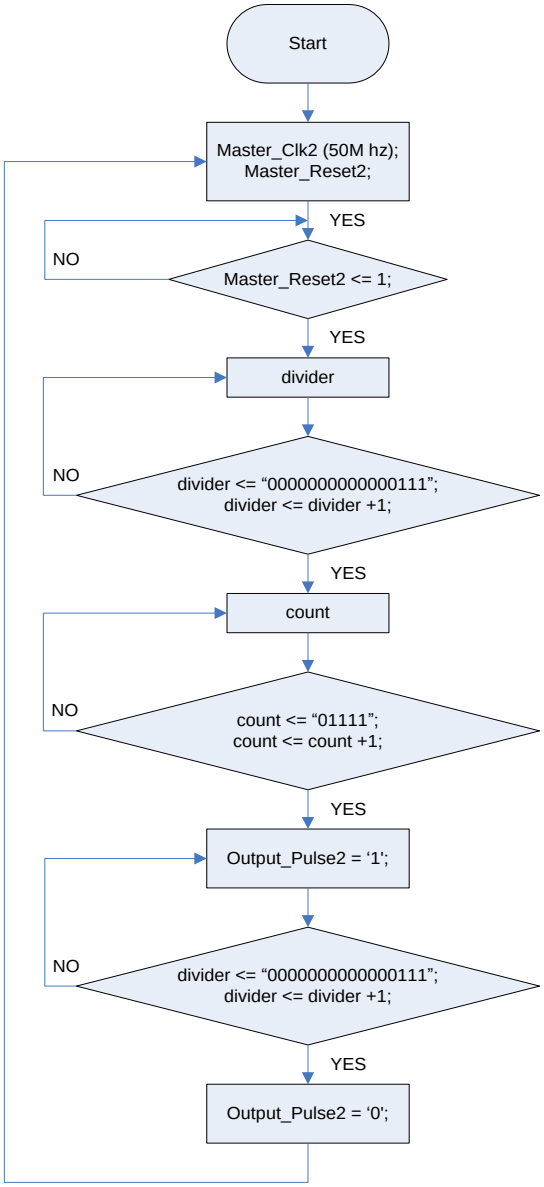

Fig. 5. Flowchart of Pulse Generator

Fig. 6a shows the module and fig. 6b shows the Register Transfer Level (RTL) for Pulse Generator. This RTL is simulated by Quartus II Design Software.

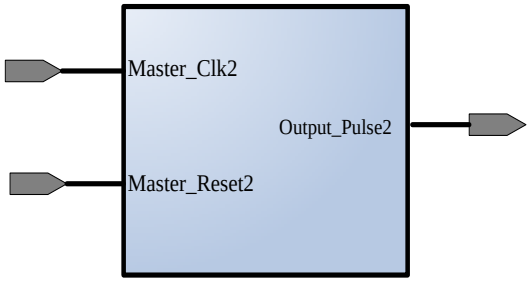

Fig. 6a. Module of Pulse Generator

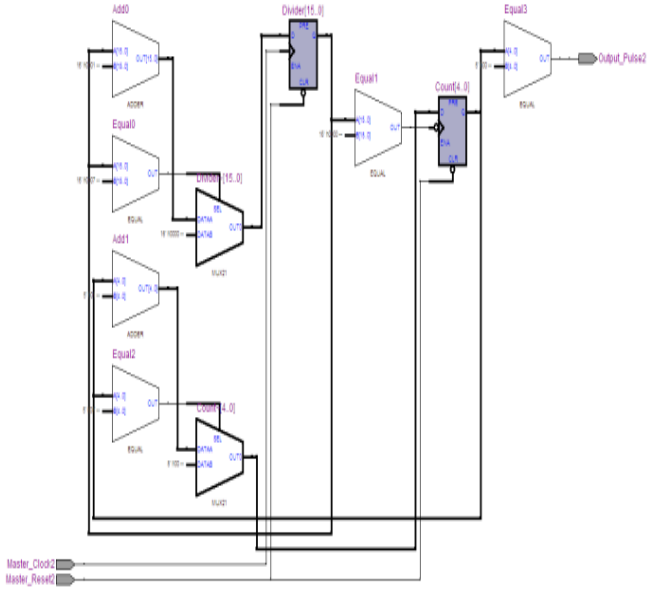

Fig. 6b. RTL of Pulse Generator

B. *Demultiplexer 1:16*

The opposite of the multiplexer is the demultiplexer (demux). This circuit takes a single data input and one or more address inputs, and selects which of multiple outputs will receive the input signal. Demultiplexer 1:16 is used as the process of separating the pulse generator signal to each pilot cable that been test. The idea is to inject pulse into pilot cable one by one. For this project, only 10 outputs been used due to decade counter. Fig. 7 shows the simulation result of demux 1:16 while Fig. 8 show the RTL for demux 1:16.

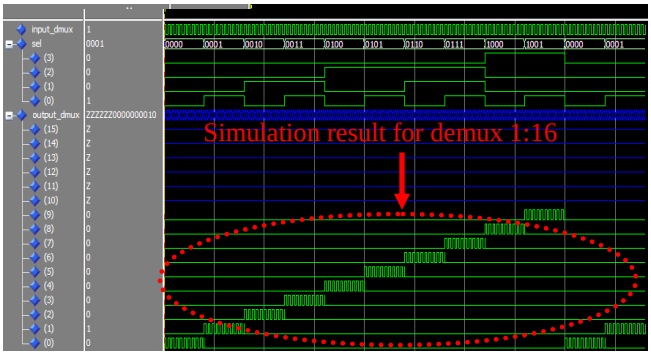

Fig. 7. Simulation Result for Demux 1:16

Fig. 8a show the module and Fig. 8b show the Register Transfer Level (RTL) for Demux. This module and RTL is simulated by Quartus II Design Software.

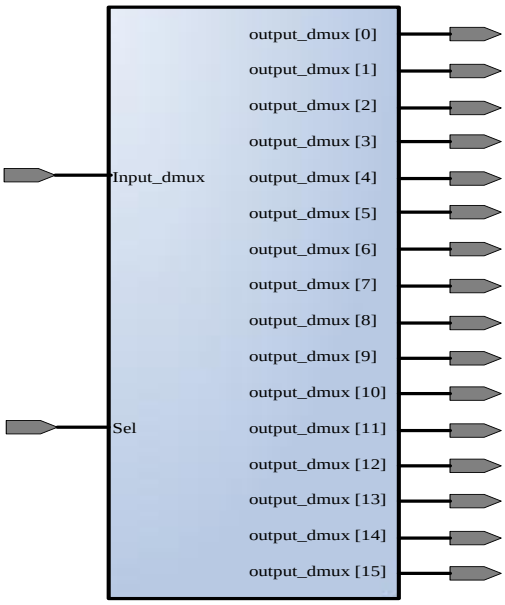

Fig. 8a. Module of Demux 1:16

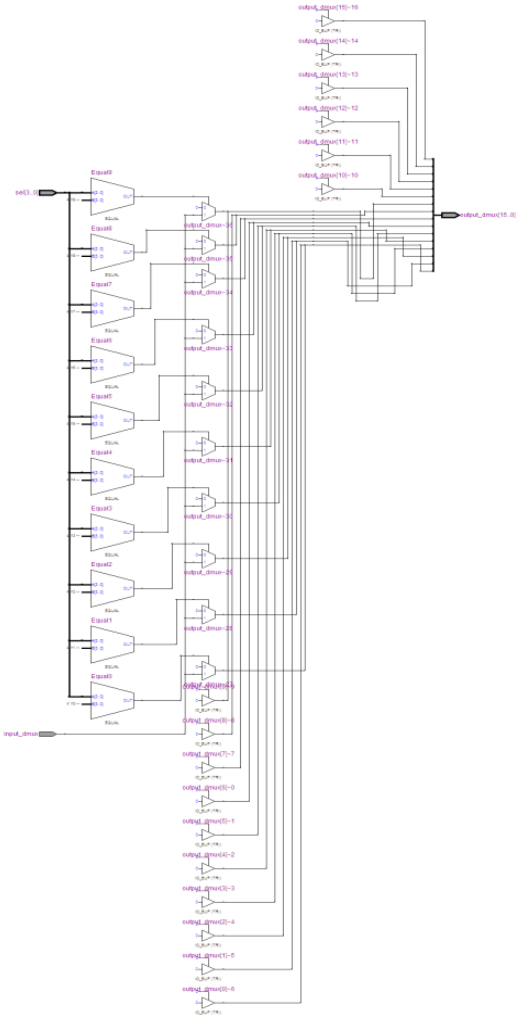

Fig. 8b. RTL for Demux 1:16

C. *Decade Counter*

Decade counter is a binary counter that designed to count to 10 which from "0000" to "1001" [3]. For this project, decade counter is used to give data to the selector of the demux. It is allowed demux to select specific output according to the specific data from decade counter. Fig. 9 shows the simulation result of decade counter while fig. 10 shows the RTL for decade counter.

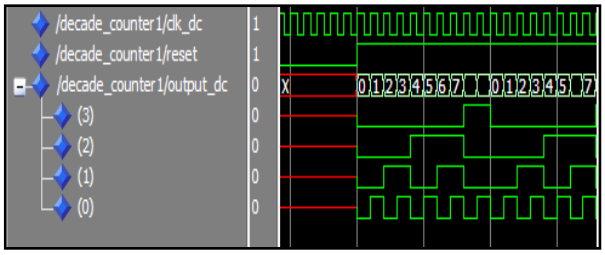

Fig. 9. Simulation Result for Decade Counter

Fig. 10a show the module and Fig. 10b show the Register Transfer Level (RTL) for Decade Counter. This module and RTL is simulated by Quartus II Design Software.

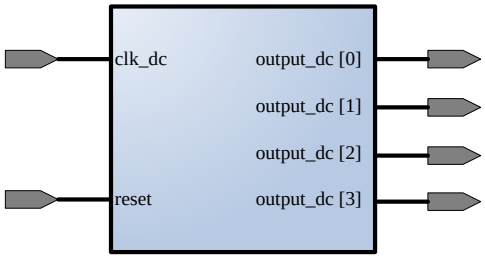

Fig. 10a. Module of Decade Counter

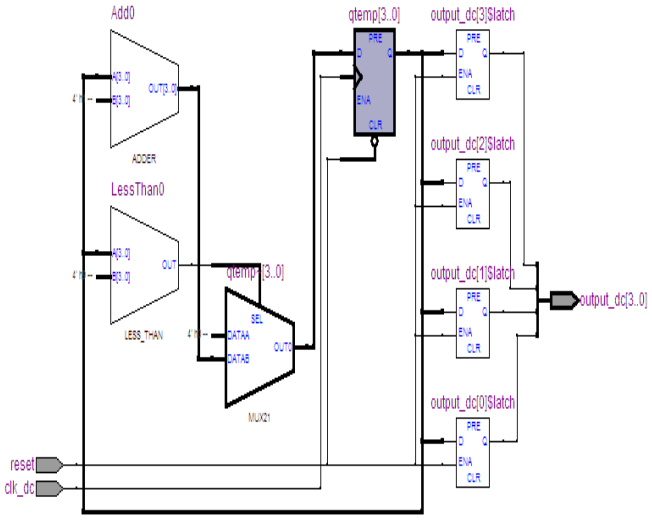

Fig. 10b. RTL for Decade Counter

D. Design for Connection between Pulse Generator, Demux 1:16 and Decade Counter

The final stage for design process is to design the connection between all modules. Fig. 11 show how the connections design between all modules.

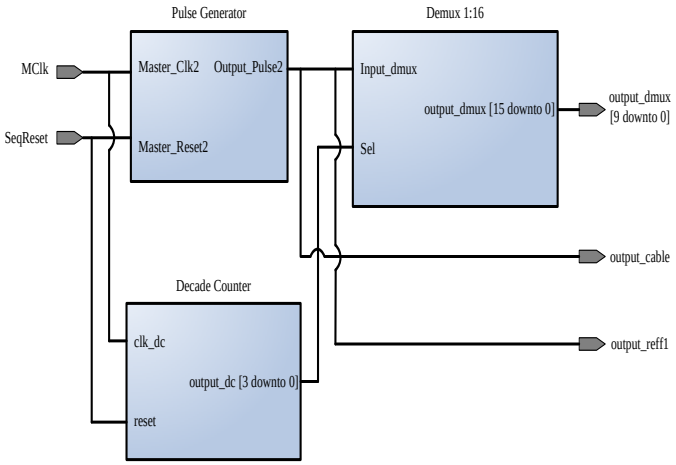

Fig. 11. Connection between Pulse Generator, Demux 1:16 and Decade Counter.

When reset (SeqReset) equal to '1' (High), ALTERA Cyclone II board generate clock (MClk) 50M hz that used to be the sensitive reference for all modules. Pulse Generator generates the pulses and sends the pulses to demux from Output_pulse2 to Input demux. Fig. 12 shows the generated pulse at the output_pulse2.

At this stage, decade counter start to count since it also sensitive to the MClk. Then outputs from decade counter (output_dc) send the data counter to the selector (sel) of the demux. The data from output_dc used to saperate the pulse to the output demux (output_dmux).

Fig. 13 shows the pulse separated to the output_dmux and the data send to the sel of demux. It repeated the process until SeqReset equal to '0' (low).

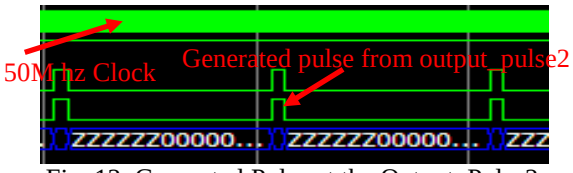

Fig. 12. Generated Pulse at the Output_Pulse2

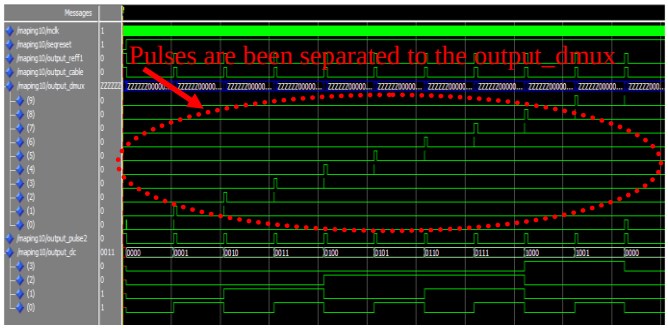

Fig. 13a. Pulse are been Separated to Output_Dmux

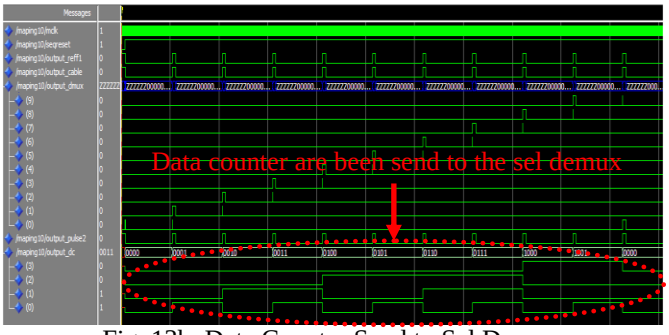

Fig. 13b. Data Counter Send to Sel Demux

Maping technique also been used for combination all three modules. At this stage, only inputs and outputs pins are shows as known as "Top Level". Input pins for this top level are MCLK and SeqReset while the output pins are output_reff1, output_cable and output_dmux. Fig. 14 shows the top level of this project.

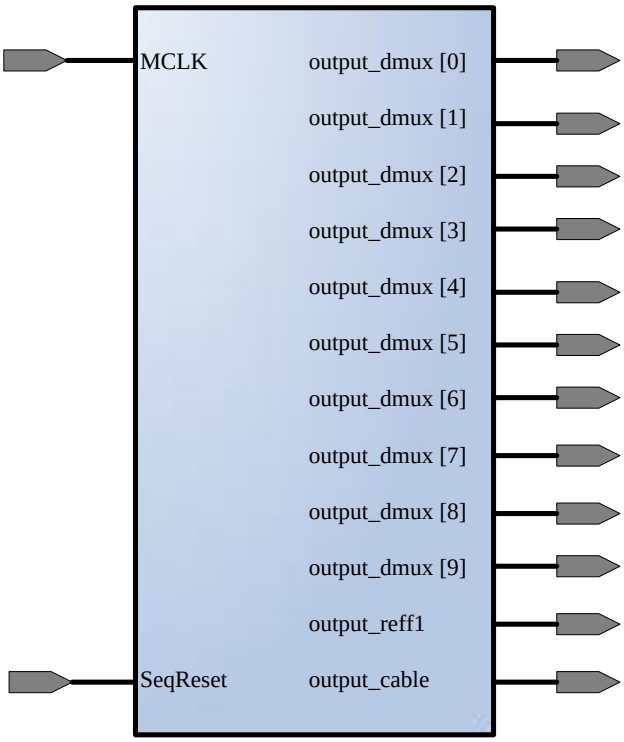

Fig. 14. Top Level Module of Faulty Pilot Cable Test

Fig. 15 shows the connection for all three modules. It shows the connection between modules that done by Quartus II Design Software.

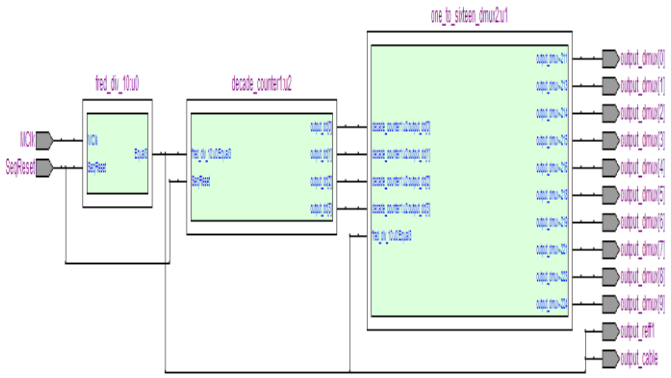

Fig. 15. Connection of Simulation for All Three Modules (Pulse Generator, Demux 1:16 and Decade Counter)

E. Testing Method

For this project, method on how to test pilot cable is critical because it will determine the result of the healthy and faulty cable. First it needs to determine the pattern of the healthy pilot cable. Several cables have to be tested randomly by injecting pulse and each of the pattern's results has to be recorded for further evaluation [4]. The healthy cable pattern will show the same reflection for all healthy cable. For confirmation of the healthy cable's distance, simple calculation shown below is needed [3].

$$D = t \times v_\rho \qquad (1)$$

Where, **D** = Distance of faulty or healthy Cable

$\mathbf{v_\rho}$ = Velocity of Propagation

t = transmit time from monitoring point measured on the oscilloscope

* For this project, the length of pilot cable being tested is 10 m and the $\mathbf{v_\rho = 0.995e^{-1}}$ **m/ns at 10 m** distance.

* The patterns illustrated here are only applicable for this project and they may change if different distance and type cables are used.

III. RESULTS AND DISCUSSION

A. Pulse Generator

For pulse generator, the results from simulation are compared with signals obtained from digital sampling oscilloscope (DSO). The pulse width for this project is 160ns with 2400ns delay between pulses.

The pulse produced from ALTERA Cyclone II board as shown in Fig. 16a-Fig.16c and they are injected to selected Pilot Cable.

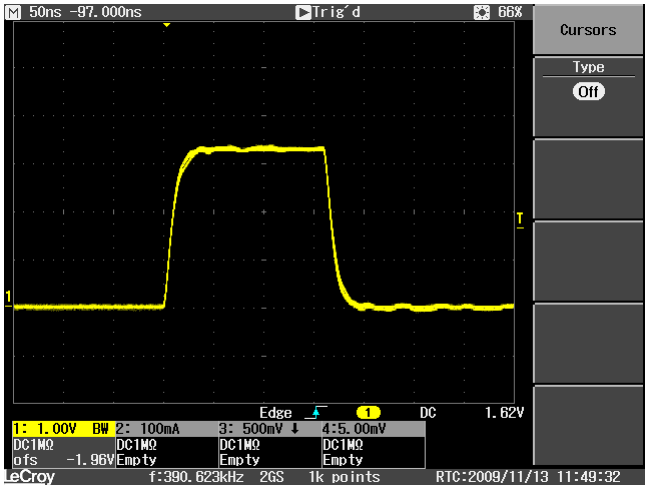

Fig. 16a. Result of Pulse Generator

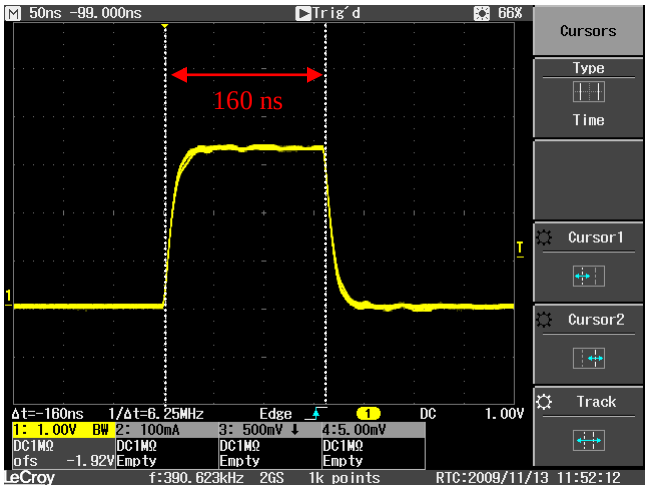

Fig. 16b. Result of 160ns Pulse Width

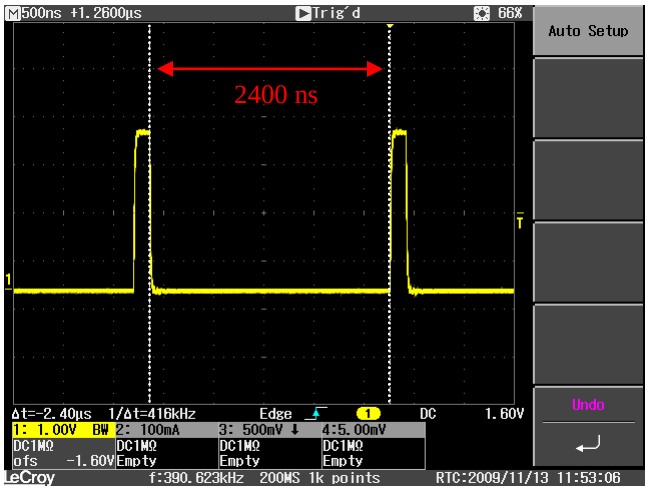

Fig. 16c. Result of 2400ns Delay between Pulses

B. Pattern of Healthy Cable

For this project, the pattern of healthy has been determined. Fig. 17 shows the TDR pattern for healthy cable. Since there is no reflection for healthy cable, so the time been measured from initial waveform to the changes of the waveform. The time has been measured and calculated by using (1). The time reflection is 100ns. Since the

$$D = t \times v_\rho$$
$$D = 100n \times 0.995e^{-1}\ m/n$$
$$D = \mathbf{9.95\ m}$$

From the calculation, it shows the length of healthy cable is 9.95m but the actual length for the cable is about 10m and this length is used for approximating the pulse width to be injected to the cables.

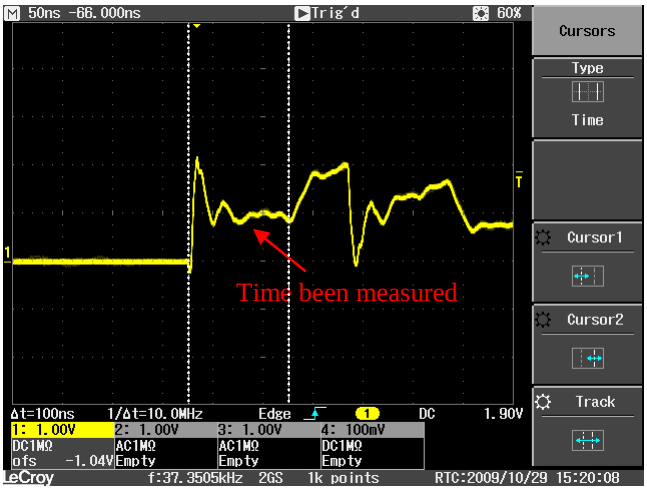

Fig. 17. TDR Measured Result and Pattern for Healthy Cable (100ns)

C. Pattern and Result Distance of Faulty Cable 1

The pattern of faulty cable1 has been determined. Fig. 18 shows the TDR pattern for faulty cable 1. For faulty cable 1, the reflection waveform pattern (step waveform) clearly illustrate in fig. 18. The time reflection has been measured and calculates by using (1). The time reflection is 36ns.

$$D = t \times v_\rho$$
$$D = 37n \times 0.995e^{-1}\ m/n$$
$$D = \mathbf{3.582\ m}$$

From the calculation, it shows the length of faulty cable 1 is 3.582m.

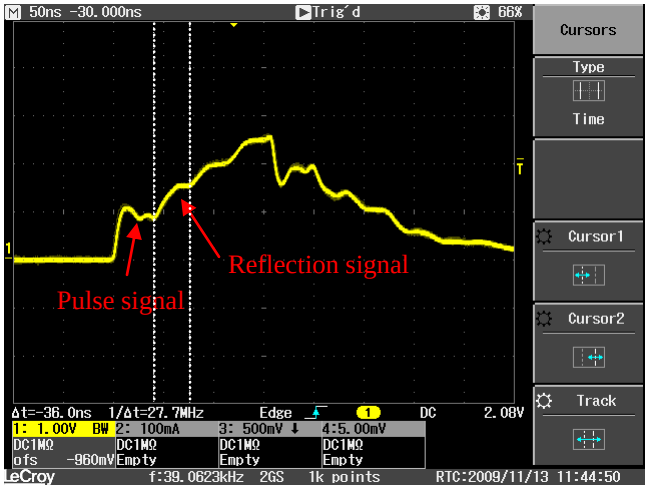

Fig. 18. TDR Measured Result and Pattern for Faulty Cable (36ns)

D. Pattern and Result Distance of Faulty Cable 2

The pattern of faulty cable 2 has been determined. Fig. 19 shows the TDR pattern for faulty cable 2. The time reflection has been measured and calculates by using (1). The time reflection is 51ns.

$$D = t \times v_\rho$$
$$D = 51n \times 0.995e^{-1}\ m/n$$
$$D = \mathbf{5.075\ m}$$

From the calculation, it shows the length of faulty cable 1 is 5.075m.

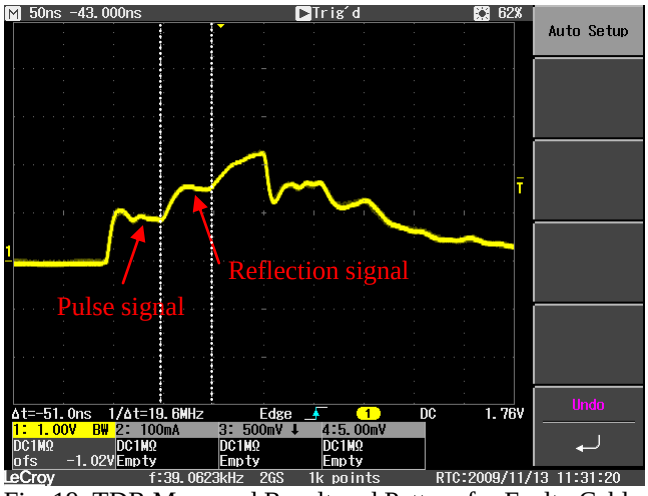

Fig. 19. TDR Measured Result and Pattern for Faulty Cable (51ns)

E. Comparison Result

Table 5.1 shows the comparison result between all measurements. For healthy cable, the result for this project is 9.95m and the actual distance cable is 10m. Its shows that result from this project are similar to the actual distance cable. For this project, the accuracy distance is 99.5% accurate.

For faulty cable 1, the result for this project is 3.582m and the actual distance is 3.6m. The accuracy distance for faulty cable 1 is 99.5%. For faulty cable 2, the result distance for this project is 5.075m and the actual result is 5m. The accuracy of faulty cable 2 is 98.5%.

From the result, the accuracy for this project is about 99.17%. Its mean, the tolerant for this project is ±1%.

Description	Time Measured (ns)	Calculation Distance D = t X Vp (m)	Actual Distance (m)	Accuracy Distance
Healthy Cable	100	9.95	10	99.5%
Faulty Cable 1	36	3.582	3.6	99.5%
Faulty Cable 2	51	5.075	5	98.5%

Table 1: Comparison Result

IV. CONCLUSION

The objective of this project is to propose a digital design and technique that efficient and accurate that can detect the fault at the pilot cable without required high maintenance cost by replacing the fault pilot cable. The design module is able to detect the fault and what type of fault. The injected pulse radiates down the cable and at the point where the cable end some portion of signal of the signal pulse is reflected back to the injection point. The amount of the reflected is a function of condition at the end of the cable. In addition to the amount of energy, can analyze the reflected signal waveform and timing detail to get information on what kind of impedance mismatches can be and where they are located in the cable.

1. If the cable is in an open condition the energy pulse reflected back is a significant portion of the injected signal in the same polarity as the injected pulse.
2. If the other end of the cable is shorted to ground or to the return cable, the energy reflected is in opposite polarity to the injected signal.

The ALTERA Cyclone II board generates the pulse consistently then can be injected to the cable. With digital design, the amplitude of reflected signal can be reduced. The digital design will cause the amplitude of reflected signal not exceed more than 3V.

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