UNIVERSITI TEKNOLOGI MARA

DESIGNING AND OPTIMIZING CARBON NANOTUBE FIELD EFFECT TRANSISTOR USING TAGUCHI METHOD AND THE CIRCUIT PERFORMANCE ANALYSIS

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ABSTRACT

The 2022 IRDS emphasized CNTFET as a CMOS replacement. Thus, further optimizing the CNTFET physical parameter is a must to provide a better performance in circuit application. However, changing physical parameters might involve trade-offs between performance and reliability of the CNTFET. For instance, while reducing the diameter of Carbon Nanotube (CNT) might reduce power consumption of the applied circuit, but the changes could simultaneously compromise its propagation delay. Balancing these trade-offs to achieve both high performance and reduce reliability is a critical challenge. Thus, this study involves designing the geometrical structure of CNTFETs that can provide the best combination on CNTFET parameter that can produce the best performance towards circuit application. Through simulations and analysis, the study examines the impact of various geometrical parameters on device performance. Parameters such as diameter of CNT, oxide thickness and dielectric materials are varied to explore their effects on CNTFET behaviour, enabling a deeper understanding of the device's characteristics. Several response variables can be extracted from the simulation such as current ratio (I_{on}/I_{off}), subthreshold slope (SS), Drain-Induced Barrier Lowering (DIBL) and threshold voltage (V_{th}). In this design, the Taguchi method was implemented to determine the best combination of design parameter and material for optimum CNTFET performance. The design parameter and material that had been chosen were the diameter of carbon nanotube (D_{cnt}), dielectric material and oxide thickness (t_{ox}). The best combination to produce the optimum current ratio for CNTFET are the transistor with the 4.0 nm of CNT diameter, 2.0 nm of oxide thickness and TiO2 (dielectric constant, K=80) as the dielectric material. The similar optimization method is implemented in Cadence Virtuoso software using the Stanford University CNTFET model. The optimized CNTFET model is implemented in circuit study to analyse the propagation delay and power consumption. Five circuit had been designed from the optimized CNTFET which are the inverter, AND, OR, NAND and NOR circuit. The data demonstrates that the Taguchi Optimization approach consistently outperforms the model across various circuits from previous research. The power delay product (PDP) for the optimized CNTFET experiences significant reductions with Taguchi method implementation. These findings indicate that Taguchi method offers substantial improvements in power efficiency and circuit speed, highlighting its potential for energy-efficient and high-speed circuit design.

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CHAPTER ONE
INTRODUCTION

1.1 Research Background

Technology today develops and grows rapidly as time goes by. To keep up the positive trend, the semiconductor and microelectronic industry practiced Moore's Law to produce better technology. Moore's Law states that for every 24 months, the number of transistors on a chip doubles its number [1]. This law caused every company involved in the semiconductor and microelectronic industry to compete to achieve a better performance device and meet every demand in present society. To achieve the requirement, the industry has pushed the shrinking of MOSFET for the past 5 decades [2]. The shrinking of MOSFET enables more transistors can be installed into one single chip with an improved circuit performance which can perform more functionality [3]. By continuously following Moore's Law, the MOSFET technology may reach its limit. Further downscaling MOSFET below 10 nm shows some limitations due to intrinsic device characteristics [4][5]. The limitation faced by the MOSFET technology is the short channel effect (SCE). SCE phenomenon will lead to other issues such as the hot carrier effect, drain-induced barrier lowering (DIBL), and subthreshold leakage current [6][7].

The decreasing feature size of MOSFET devices is accompanied by an increase in the electric field in their channel regions. Hot carriers are charged particles, either electrons or holes. These include particles that have acquired very high kinetic energies upon acceleration by the large electric field prevalent across the channels of MOSFETs. These carriers have higher energies than those of carriers normally found in semiconductor devices. Due to their high energies, hot carriers may migrate into and roam around the unwelcome areas of the devices [6]. Such areas are the gate dielectric and substrate of a transistor. They cause shifts in threshold voltage. Device transconductance is also degraded.

Ideally in MOSFET models is expected to have current equal to 0 for Vgs = 0, however in reality there is still a flow of current in the gate terminal. This current is