

Four Quadrants DC to DC Converter Using Single Phase Matrix Converter Topology

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Abstract—This paper presents a single phase matrix converter topology (SPMC) as a DC chopper (DC-DC) controlled using Xilinx Field Programmable Gate Array (FPGA). Insulated Gate Bipolar Transistor (IGBT) was used for its power circuits, with Xilinx FPGA at heart of its digital control implementations. Pulse Width Modulation (PWM) technique was used to calculate the switch duty ratio to synthesize the DC output. Computer simulation model was developed using MATLAB/Simulink (MLS) to study the basic behavior. Safe commutation strategies were developed through an arrangement of commutation switches that allows dead time to avoid voltage spikes due to inductive load. Experimental Test-Rig was constructed to verify the operation. Selected simulation and experimental results are presented to verify proposed operation.

Keywords: DC Chopper, Single Phase Matrix Converter (SPMC), Pulse Width Modulation (PWM), Safe commutation, Insulated Gate Bipolar Transistor (IGBT), Field Programmable Gate Array (FPGA), MATLAB/Simulink (MLS).

I. INTRODUCTION

A chopper circuit is used to refer to numerous types of electronic switching devices and circuits. The term has become somewhat ill-defined, and as a result is much less used nowadays than it was perhaps 30 or more years ago^[2]. Usually, a chopper is an electronic switch that is used to interrupt one signal under the control of another. Few example of chopper application such:

- Switched mode power supplies, including DC to DC converters.
- Speed controllers for DC motors
- Class D Electronic amplifiers
- Switched capacitor filters
- Variable Frequency Driver

Choppers are widely used for traction motor control in electric automobiles and other electric transportation system. In those applications, control of DC motor's speed is required

where the supply is DC or an AC voltage that has been rectified. Other applications of DC chopper also include high-current DC applications in industries which have many operational benefits over conventional diode or thyristor^[1].

The Matrix Converter (MC) is a modern and advanced power conversion topology which was first introduced by Gyugyi (1976) [1]. It offers possible "all silicon" solutions, unrestricted switch control, minimal and removing the need for reactive device use in conventional converter system [2]. Therefore the size of the converter can be reduced since there are no large reactive components for energy storage [3]. It has possibility of greater power density due to the absence of a DC link [4] in direct AC conversion.

Besides, matrix converter is able to operate in the all four quadrants operation. These features make the matrix converter a suitable alternative to the traditional DC chopper. This matrix converter present future potential and become emerging research topic. Previous studies are focused on Three-Phase Matrix Converter (TPMC) topologies which the concepts were first introduced by Alesina and Venturini in 1980 [3,6]. They represent the circuit as matrix of bi-directional power switches. It is a force commutated converter which uses an array of controlled bidirectional switches as the main power elements to create a variable output voltage system with unrestricted frequency.

The SPMC topology although offering very wide application but has very little attention. The SPMC was first proposed by Abdullah Khoei et al [7] without relating to matrix converter and any operation details. It was first described as a single phase matrix converter and realized by Zuckerberger et al [8] in 1997 using MOSFETs as switching device. Other SPMC studies include works on DC-AC (Inverter) by Hosseini *et al.* [9] in 2001, AC-AC by Saiful *et al.* [10] in 2002 and DC-DC conversion by Siti Zaliha Mohd Noor [11] in 2005.

This paper will discuss the design and development of Pulse-Width Modulation (PWM) generator suitable for SPMC operating as a DC chopper. It is based on the Xilinx chip XC4005XL FPGA with IGBTs as the power switching device. The output voltage is synthesized using Pulse Width Modulation (PWM). The proposed design enables the modulation index and the switching frequency to be changed externally. The experimental result from hardware implementation will be compared with those simulations using Matlab Simulink to verify proposed operation.

II. CLASSICAL DC TO DC CONVERTER

Single-phase DC-DC converters are used in a great variety of applications such as controlling DC motors for household or industrial use (e.g., in washing machines, refrigerators, dishwashers, industrial machines). Classical DC-DC converter normally uses bridge-diode without affording any control function and is unidirectional in nature [14]. Bidirectional operation is also possible with the inclusion of anti-parallel switch in H-bridge topology of Figure but is not fully controllable.

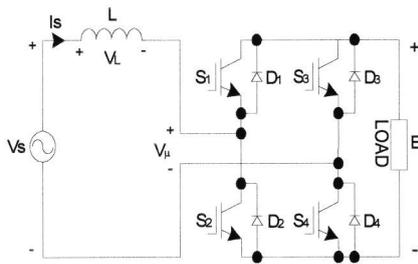


Figure1: H-Bridge Topology.

III. SINGLE PHASE MATRIX CONVERTER

Basically, SPMC used in direct AC-AC converter that requires four bi-directional switches as shown in Figure 2 each capable of blocking voltage and conducting current in both directions. Unfortunately no discrete semiconductor device currently could fulfill the needs [12,13], therefore common emitter anti-parallel IGBT and diode pair was used as shown in figure 2 making the module capable of bidirectional operation. The IGBT were used due to its popularity amongst researchers that could lead to high-power applications with reasonably fast switching frequency for fine control.

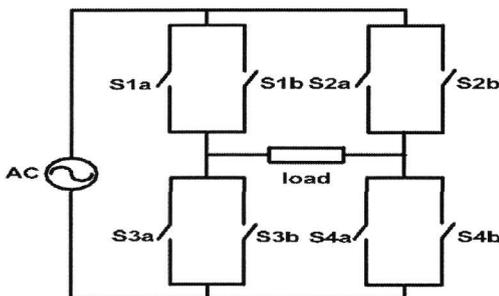


Figure 8: AC-AC single-phase matrix converter topology

Theoretically the switching sequence in the SPMC must be instantaneous and simultaneous; unfortunately impossible for practical realization due to the turn-off IGBT characteristic, where the tailing-off of the collector current will create a short circuit with the next switch turn-on. This problem occurs when inductive loads are used. A change in current due to PWM switching will result in current and voltage spikes being generated resulting in the occurrence of a dual situation. First current spikes will be generated in the short-circuit path and secondly voltage spikes will be induced as a result of change in current direction across the inductance. Both will destroy the switches in use due to stress. A systematic switching sequence is required that allows for the energy flowing in the IGBT's to decay in a free-wheel manner.

In conventional dc chopper, the free-wheeling diode is used to this purpose. In SPMC this does not exist, hence a switching sequence needs to be developed to allow forced on controlled free-wheeling. This is to protect the converter from being damaged as a result of voltage and current spikes as described. In conventional converter this is normally implemented in the form of free-wheeling diodes in inverter systems arranged in anti-parallel with power switching devices. In this study, we will focus our attention to switching spikes and assume that there is no-change in the direction of current so as to minimize the complexities. The use of Pulse Width Modulation as in figure 3 as the switching algorithm in this converter, results with possible reversal current if inductive loads are used, during switch turn-off. Detailed treatment on safe-commutation problem can be obtained in reference [18] restated here briefly for completeness.

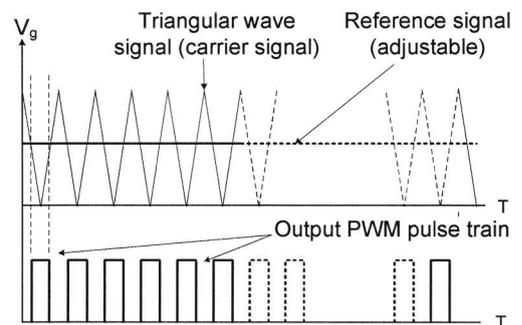


Figure 3: Pulse Width Modulation

IV. PROPOSED FOUR QUADRANT DC TO DC CONVERTER

The implementation of the SPMC as a dc chopper requires different bi-directional switching arrangements depending on the desired operational requirements of the four quadrants defined. The magnitude of the output voltage of the converter is controlled by PWM variations in duty cycle. The switching sequences are designed to follow Table 1. Figs.8 to 11 illustrates the four quadrant operation of dc chopper using SPMC topology. The dotted line flow of current in the diagram represents the safe commutation switch during each particular state that is continuously turned-on as in Table 1. The dark arrow on the switch indicates that the switch is turned-on and behaves as the power switches performing the required converter operation.

Table 1: Switching pattern for four quadrant dc to dc matrix converter

Switches	First Quadrant	Second Quadrant	Third Quadrant	Forth Quadrant
S1a	Modulate	Off	Off	Off
S1b	Off	Continuously On	Off	Off
S2a	Off	Off	Modulate	Off
S2b	Off	Off	Off	Continuously On
S3a	Off	Switching	Continuously On	Off
S3b	Continuously On	Off	Off	Continuously On
S4a	Continuously On	Off	Off	Switching
S4b	Off	Continuously On	Continuously On	Off

a) First Quadrant (Q1)

The loads current are positive as shown in figure 4. The load current flows from the supply to the load. To achieve this condition, S1a and S4a are turned-on and act as a power switch performing the required converter operation synthesizing the output dependent on the control algorithm being developed. During turn-off of S1a, switches S3b and S4a are maintained as continuously ON during the cycle to complete the loop for the current return and acts in conjunction with S3b to provide the free-wheel operation whenever S1a is turn OFF.

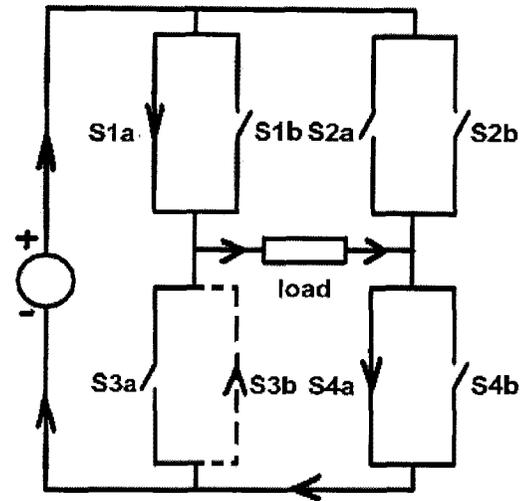


Figure 4: First Quadrant

b) Second Quadrant (Q2)

The load voltage is positive with negative load current as shown in figure 5. The loads current flows out of the load. To achieve this condition, Switch S3a and S4b will operate while S1b will be continuously turned-on, the voltage E will drives current through the load and when both switch S3a and S4b are turn OFF, load dissipates energy through S1b to the supply.

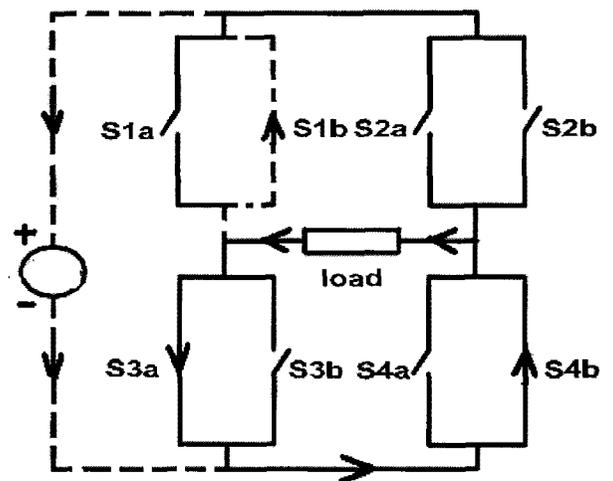


Figure 5: Second Quadrant

c) Third Quadrant

The load voltage and load current are negative as shown in figure 6. It is the reverse of first quadrant, where the load current flows from the supply to the load through a different route. To achieve this condition, S2a and S3a are turned-on and act as a power switch performing the required converter operation synthesizing the output dependent on the control algorithm being developed. During turn-off of S2a, switches S3a and S4b are maintained as continuously ON during this cycle; S3a to complete the loop for current return and acts in conjunction with S4b to provide free-wheel operation whenever S2a is turned OFF.

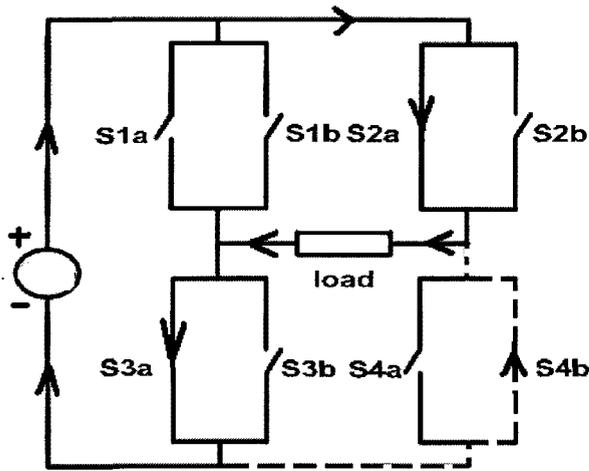


Figure 6. Third quadrant

d) Third Quadrant

In the fourth quadrant, the load voltage is negative but the load current is positive as shown in figure 7. The loads current flows out of the load. To achieve this condition, Switch S3a and S4b will operate while S1b will be continuously turned-on, the voltage E will drives current through the load and when both switch S3a and S4b are turn off, load dissipates energy through S1b to the supply

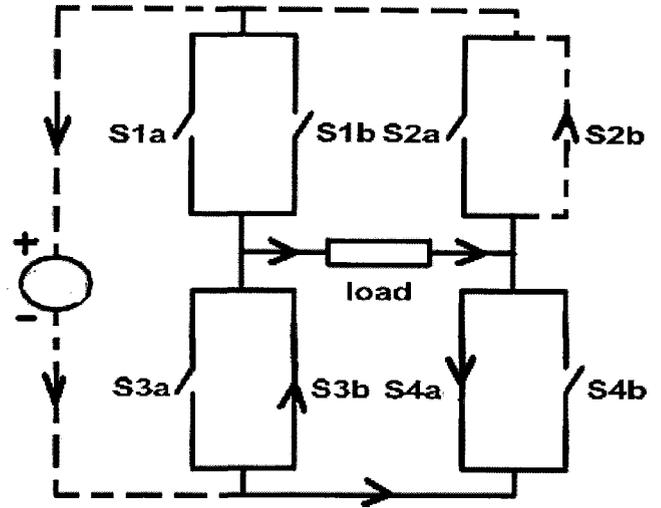


Figure 7: Forth quadrant

V. MODELLING AND SIMULATION

MATLAB Simulink (MLS) is used as simulation tool to study the behavior of the rectifier operation. Figure 8 shows the top level main model of the SPMC. The subsystems are as shown in Figure 9 and 10.

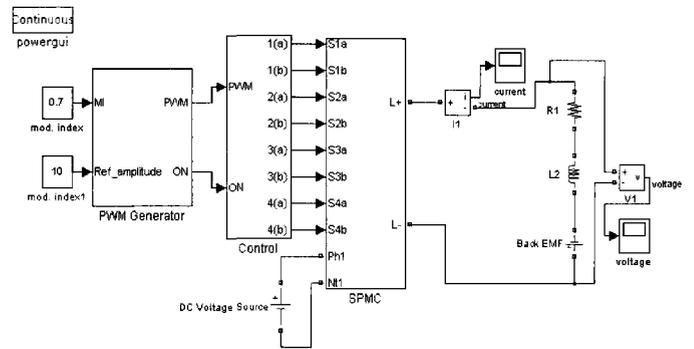


Figure 8: Top level main model of DC Chopper

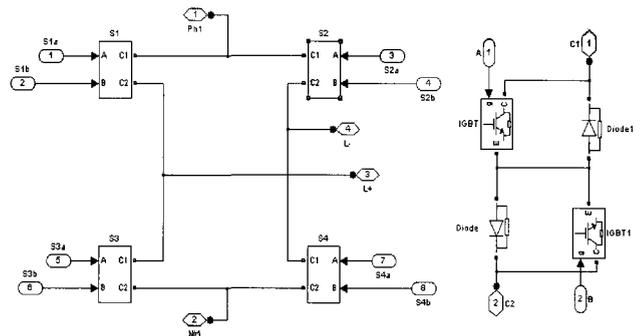


Figure 9: (a) SPMC Model in MLS and (b) Bidirectional switch module

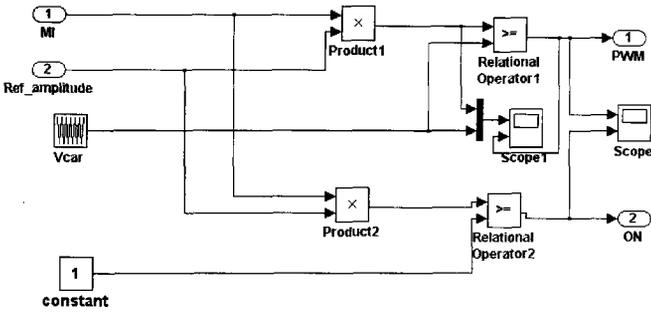


Figure 10: PWM generator model

VI. XILINX FPGA IMPLEMENTATION

There are four major components included in FPGA PWM generator design which is 1) External Main Clock, 2) 'W' shape carrier signal, 3) Comparator and 4) Modulation Index. The overall block diagram of the PWM generator in FPGA is as shown in Figure 11 and schematic diagram of XILINX FPGA DC Chopper is as shown in Figure 12. Actually PWM signal generate by comparing the triangular wave signal with the dc reference signal which can be adjusted to get the Pulse Width Modulation algorithm. An external main clock was used as the clocking signal for the FPGA counter. For this work, 5 KHz carrier signal was used. The toggle flip-flop, FTC is used to counts and changes the counting direction of the up-down counter. The counter start counting from 0 to 255 when the reset signal, 'RST' is received and it will count back to 0. This process will produce 'M' shape carrier signal as illustrated in figure 13. Inverter, INV8 was used to change 'M' shape to 'W' shape. This triangular 'W' shape then will be compared with the modulation index by using eight bit comparator, COMPM8 and will produce PWM pattern. The OR and AND gate are used in the switch selector to ensure that the PWM pulse follows the switching sequence as in Table 1.

$$= \text{---} \quad (1)$$

$$= \text{---} \quad (2)$$

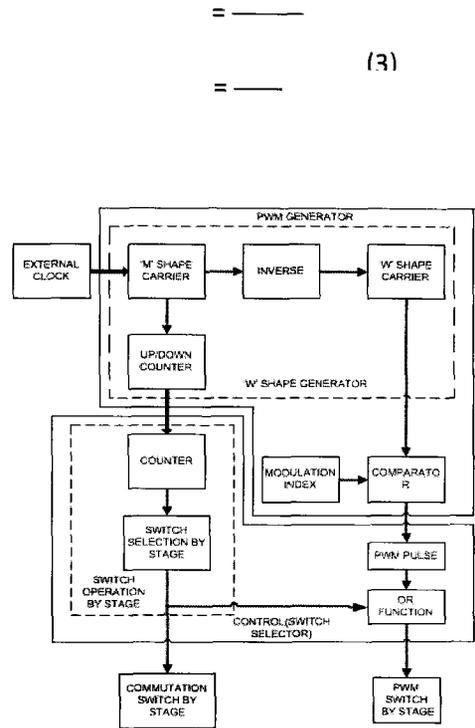


Figure 11: PWN Generator Block Diagram

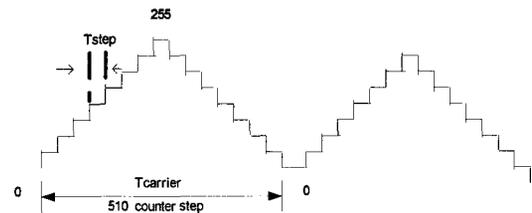


Figure 13: 'M' shape carrier signal

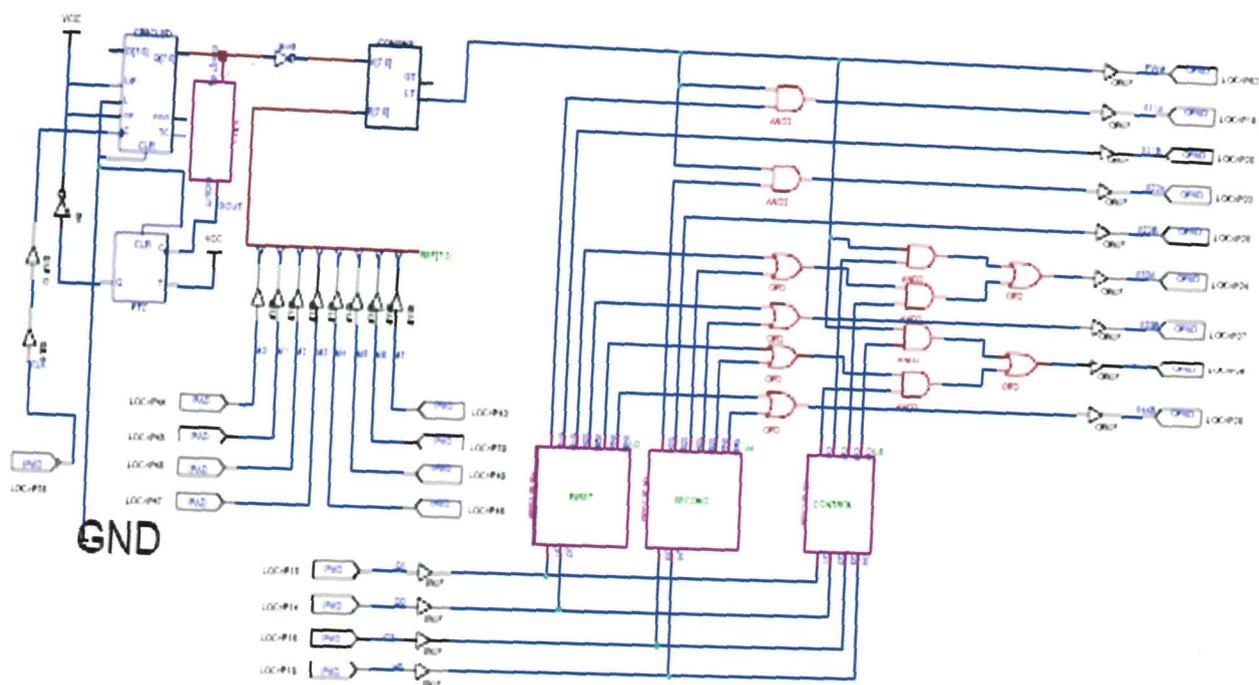


Figure 12: XILINX FPGA DC Chopper

VII. RESULT AND DICUSSION

The result of DC Chopper modeling for first and third quadrant operation is shown in figure below. From the simulation result, the four-quadrant dc-to-dc converter can be modeled and implementation by using the MATLAB/Simulink. The switching techniques and controlled strategies need to implement carefully to make sure that this power converter operated as needed.

When the modulation index is increased from 0.1 to 1.0, turn-on width will be increased in steps of 10% of the modulation index. This variation is independent on the quadrant of operation; which only effects the polarities of voltage and current.

Figure 14 until figure 25 shows the variations of mean voltage and current with respect to modulation index, MI. Mean Voltage and current increased non-linear with the variation of modulation index maybe due to low values of voltage used resulting in higher possible inaccuracies in measurements. Modulation index 1.0 gives the highest mean voltage and current output.

a) V_{mean} of the first quadrant with R load at 3kHz

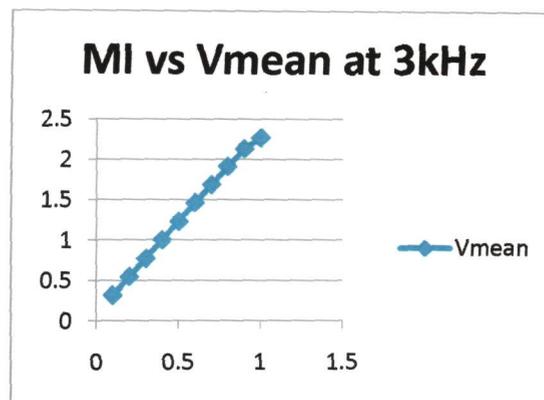


Figure 14

b) I_{mean} of the first quadrant with R load at 3kHz

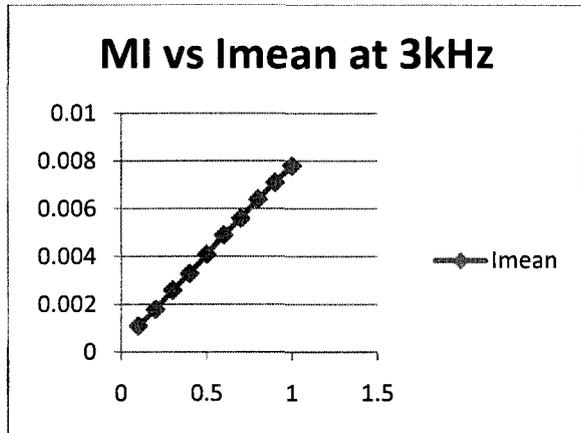


Figure 15

c) V_{mean} of the first quadrant with RL load and Eb at 3kHz

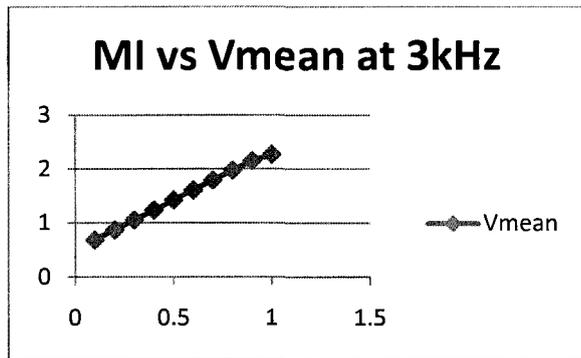


Figure 16

d) I_{mean} of the first quadrant with RL load and Eb at 3kHz

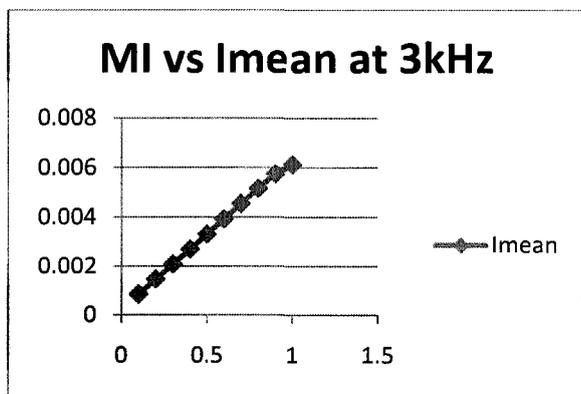


Figure 17

In quadrant 1, the load voltage is positive, $+V_L$ and the load current is positive, $+I_L$ and the current is conducting continuously.

e) V_{mean} of the second quadrant with RL and Eb load at 3kHz

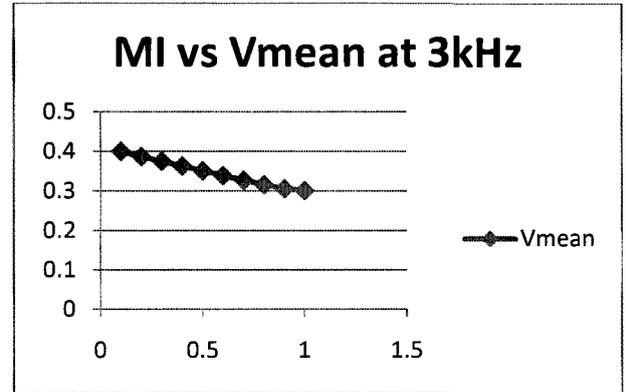


Figure 18

f) I_{mean} of the second quadrant with RL and Eb load at 3kHz

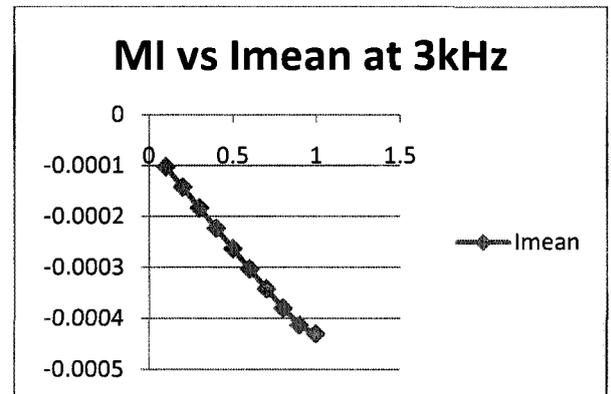


Figure 19

In quadrant 2, the load voltage is positive, $+V_L$ and the load current is negative, $-I_L$ and the current is conducting continuously.

g) Vmean of the third quadrant with R load at 3kHz

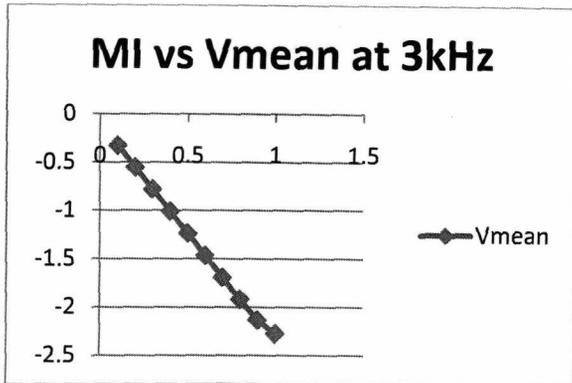


Figure 20

j) Imean of the third quadrant with RL and Eb load at 3kHz

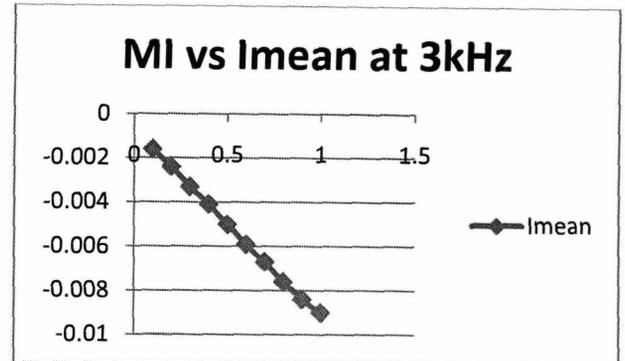


Figure 23

h) Imean of the third quadrant with R load at 3kHz

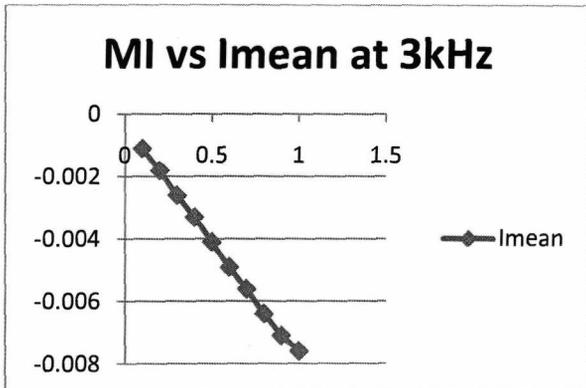


Figure 21

In quadrant 3, the load voltage is negative, $-V_L$ and the load current is negative, $-I_L$ and the current is conducting continuously.

k) Vmean of the fourth quadrant with RL and Eb load at 3kHz

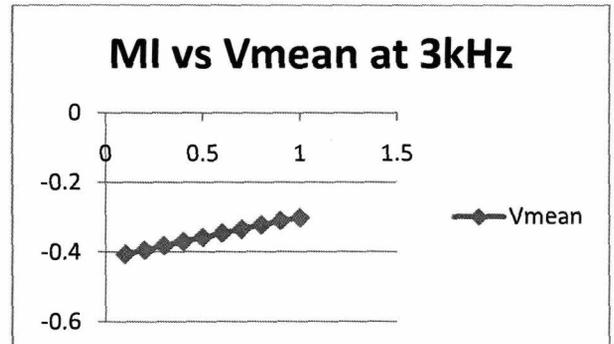


Figure 24

i) Vmean of the third quadrant with RL and Eb load at 3kHz

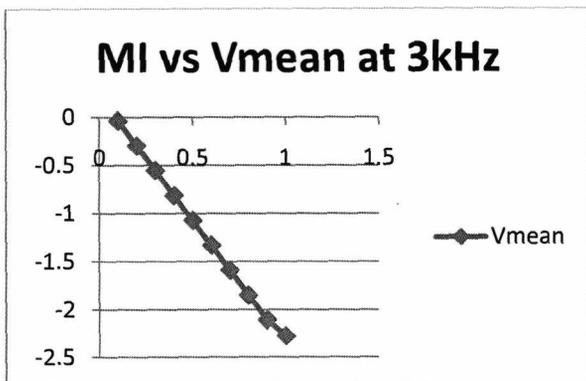


Figure 22

l) I_{mean} of the forth quadrant with RL and Eb load at 3kHz

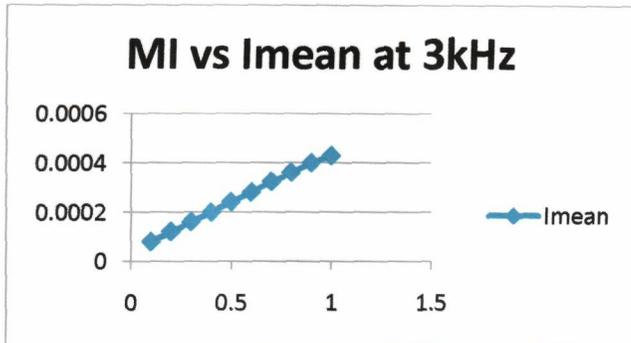


Figure 25

In quadrant 4, the load voltage is negative, $-V_L$ and the load current is positive, $+I_L$ and the current is conducting continuously.

And from figure 26 and 27, the graph obtained show that when the f_s increased, the output voltage and current increased.

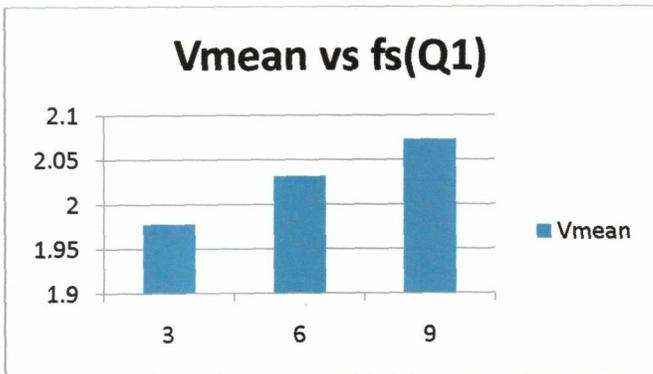


Figure 26

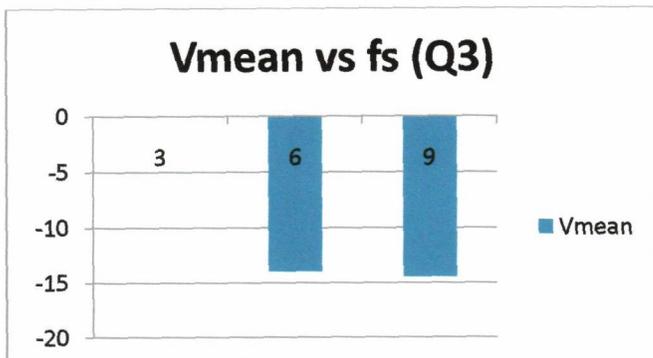


Figure 27

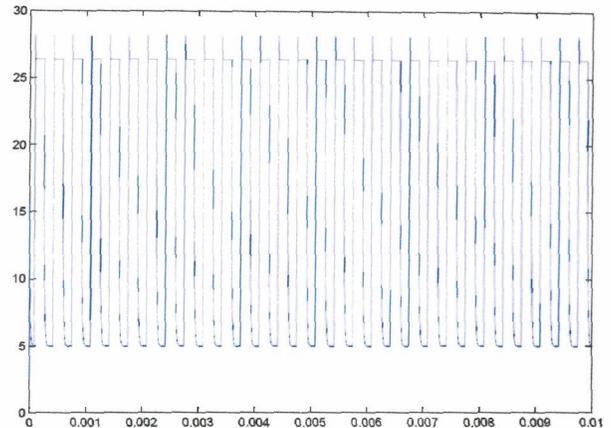


Figure 28: The output voltage produce from the first quadrant

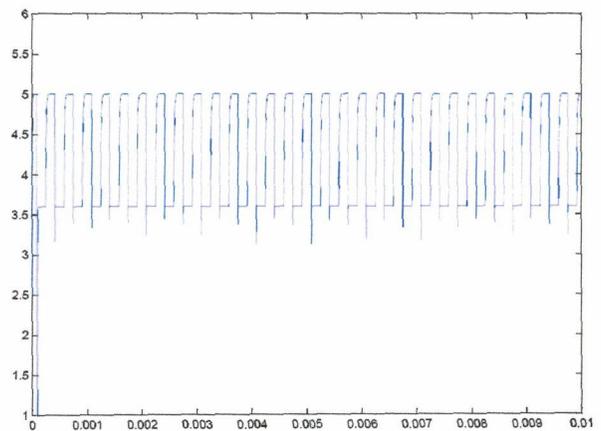


Figure 29: The output voltage produce from the second quadrant

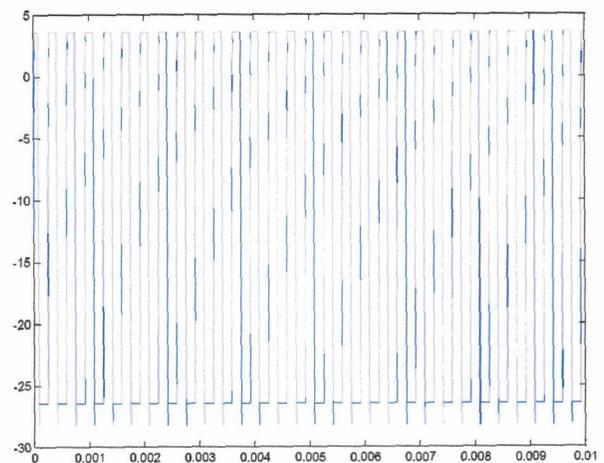


Figure 30: The output voltage produce from the third quadrant

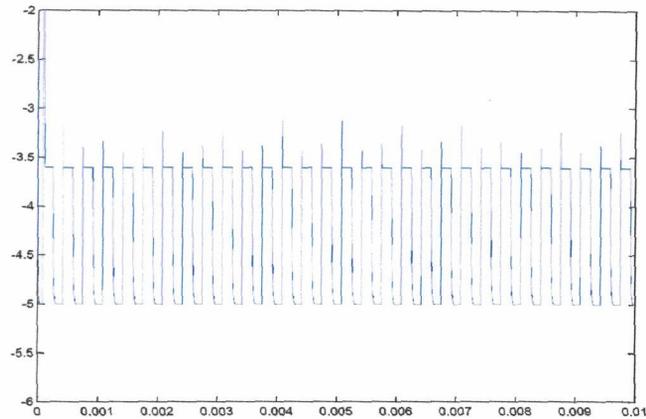


Figure 31: The output voltage produce from the forth quadrant

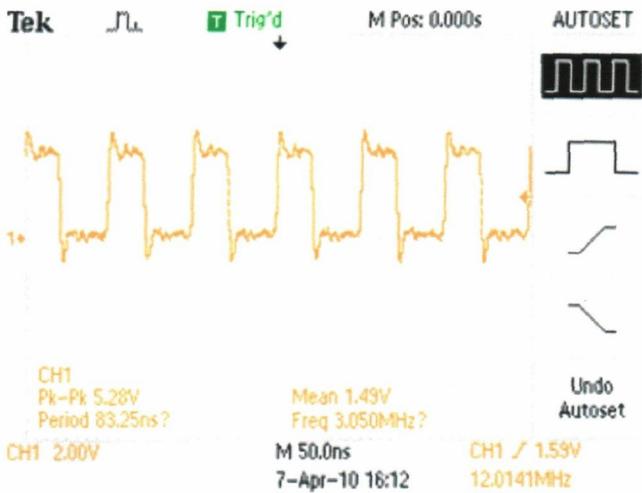


Figure 32: The PWN produces from the XILINX

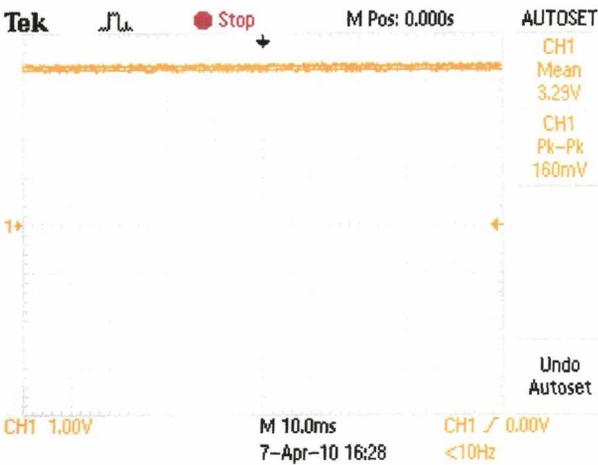


Figure 34: The constant output produces by the XILINX

VIII. TROUBLESHOOTING

Since, the output of the SPMC as a DC Chopper cannot be achieve during the hardware implementation, several step have been taken to analyze the lack or problem that may contribute to the difficulties and try to overcome to achieve the desired output. Below are the actions that have been taken on investigating the problem due to the hardware misbehavior. It is present by the table 4 below.

Table 2: Actions taking to overcome the SPMC problem

Steps taken	Explanations
Check the output from Signal Generator	<ul style="list-style-type: none"> The step taken is to achieve the constant output of the Signal Generator. Since the output produces by the Signal Generator is important but sometimes it get unstable, thus the Signal Generator get replace and recalibrate to sustain the desired output signal. As a result, the desired output of the signal is achieved.
Output from Xilinx board	<ul style="list-style-type: none"> Due to some programming error, the output form Xilinx pin is not equal as the proposed switching strategies, thus reprogramming have been done and achieve the desired switching strategies.
SPMC	<ul style="list-style-type: none"> During troubleshooting the SPMC, each component that may consist in the SPMC have been recalibrated, ensured it work as state in the data sheet and follow it original characteristic. All loosen connection have been tighten and any appropriate jumpers that need to be replaced are replaced with either better or equal to the specification of the existing jumper. Since the desired output still cannot be achieve, a risky step but yet necessary is taken to troubleshoot the SPMC which by unconnected back all the connection, split the component into part and reconnect it back and hoping it may operate as desired. Unlucky, the SPMC still not function as appropriate.

IX. CONCLUSION

The performances of Single Phase Matrix Converter (SPMC) operating as DC Chopper have been presented. This topology using IGBTs as a main power switching device, with proposed safe commutation strategy used to solve the inherent commutation problem that cause switching spikes. Experience in designing the FPGA for implementation of DC Chopper using SPMC also has been presented. This works show that the FPGA could effectively be used in SPMC with the four bidirectional switching arrangements. PWM design was placed on XILINX XC4005XL FPGA chip and capable to produce PWM pattern. The DC Chopper operation with commutation strategy was successfully implemented using XILINK FPGA and experimental result was compared with simulation result.

X. RECOMMENDATION

- a) Focus on four quadrant operation in DC motor drive application for full investigations with regenerative operation capabilities.
- b) Increase voltage to normal application level.
- c) Hardware implementation with DC motor as actual load
- d) Increase the switching frequency of operation to 20 kHz a normal application level associated with the limits of standard IGBT.

XI. ACKNOLEGMENT

Author would like to express his gratitude to project supervisor Pn. Siti Zaliha M. Noor for her advice, supervising and much more, and also to anyone who involve and help in completion of this technical report.

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