High Speed and Low Power Double-Tail Comparator for ADC Application using 0.13µm Technology

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Abstract—**This project proposes design Double – Tail Comparator for analog to digital converters (ADCs) application. This design gives better performance of the comparator by minimizing the propagation delay and the power consumption. The schematic design for this proposed design is obtained using 0.13 µm technology with supply voltage of 1.8 V and the operating frequency of 800 MHz. The design is carried out using Mentor Graphics tools and Silterra 0.13 µm technology files. The schematic design and simulations is performed using Mentor Graphics Design Architect tool. At the end of this project, the proposed design results to reduce the propagation delay and the power consume for the comparator circuit which is very important issues for various applications in electronics design.**

Keywords-Analog to Digital Converters (ADCs), Double-Tail Comparator, Switching Transistor, Low Power Dissipation, Low Propagation Delay, High Speed.

I. INTRODUCTION

The quickly developing electronics industry is pushing towards high speed low power analog to digital converters (ADCs). Comparator is electronic devices which are mainly as a part of analog to digital converter. In ADC they are used for quantization process, and are mainly responsible for the delay produced and power consumed by an ADC. A high speed low power comparator is obliged to fulfill the future demand. The comparators are used in analog to digital converters (ADCs), data transmission applications, switching power regulators and many different applications. The voltages that show up at the inputs are analyzed by the comparator that creates a binary output which represents a difference between them [1].

The comparator is used in the process of converting analog to digital signal [2]. It compares two different inputs signal to produce relevant output. In most ADCs application, the comparator is the main important fundamental building blocks and the high speed comparator influences the overall performance of ADCs directly [3]. In designing a comparator, the speed, power consumption and chip area are the important factors that must be take into consideration.

There are various designs of CMOS comparator used in the ADCs application that has been developed. The pre-amplifier based comparator is the most common design of comparator. This design only applied the simple working principle of the comparator. The drawback of the pre-amplifier based comparator design is that it suffers from large static power consumption [4]. Besides, the Single-tail comparator design is widely used in analog to digital converters, with high input impedance and no static power consumption. On the other hand, the Double-tail comparator design is introduced. This architecture has two tail transistors and it is used for low power application [5].

A. Analog to Digital converter (ADCs)

Analog to digital converter (ADCs) is an electronic integrated circuit for converting a signal from analog to digital form [6]. Most of signal sensed and processed by human are analog signal such as an audio signal like microphone. The analog signals needs to be converted to the digital signals, and hence the microprocessor will be able to read and understand the data.

ADCs converts analog signal into digital data that can be processed by computers for various purposes. The main purpose of the ADCs is that to digitize the analog signals, which means to record and store the analog signals in numbers.

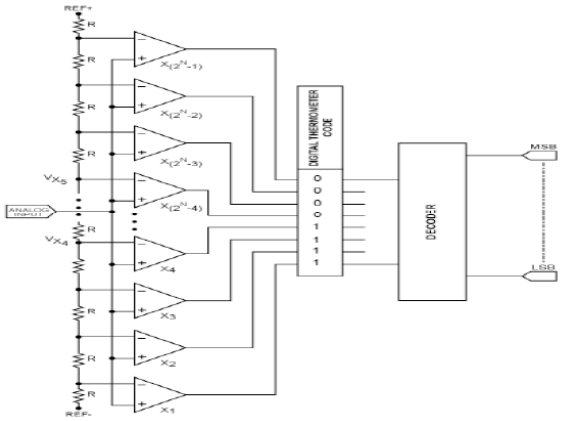

Figure 1. Flash ADCs architecture

B. Comparator

Comparator is the device that looks at two simple voltages or current and changes it output to show which one is bigger. A voltage comparator has two inputs voltage and one output voltage. It thinks about the voltages at the positive and negative inputs of the comparator. The operation of the comparator is that if the positive input is at a higher voltage than the negative input, the output will be high and if the negative input is at a higher voltage than the positive input, the output will be low.

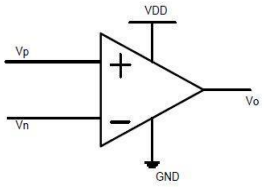

Figure 2. Schematic of comparator

A pre-amplifier based comparator for low power and high speed was discussed by Shubhara Yewale, Radheshyam Gamad et al [1]. In the design, they used four transistors (two NMOS-PMOS pair) in the inverter combination. This combination reduces the parasitic capacitance and achieved high comparison speed. The result obtained by this paper exhibit power consumption about 102 µW with operating frequency 125 MHz and 1.8 V supply.

The pre-amplifier based comparator suffers not only from large static power consumption for a large bandwidth but also from the reduced intrinsic gain with a reduction of the drain to source resistance due to the continuous technology scaling. The input-referred latch offset voltage can be reduced by using the pre-amplifier preceding the regenerative output-latch stage. It can amplify small input voltage difference to a large enough voltage to overcome the latch offset voltage and also can reduce the kickback noise [7].

Monica Rose Joy, Thangamani M. et al [5] were designed the Single – Tail and Double – Tail comparator for flash ADC circuit. The single-tail comparator was designed since they can make fast decisions due to the strong positive feedback in the regenerative latch. However, in this design structure is that there is only one current path, via tail transistor, which defines the current for both the differential amplifier and the latch (the cross-couple inverter). While one would like a small tail current to keep the differential pair in weak inversion and obtain a long integration interval, a large tail current would be desirable to enable fast regeneration in the latch. Result obtained by this comparator design exhibit power consumption about 7 µW and delay about 66 ns using 0.18 µm CMOS technology with VDD = 0.8 V.

Besides, in the double-tail design architecture that is shown in Fig. 3, there are two tail transistors exist. This design comparator is used for low power application. In this technique, it will increase the voltage difference between the output nodes in order to increase the latch generation speed. For this reason, two control transistors are added to the first stage in parallel yet in a cross-couple way. At the point when one of the control transistors turns on, a current from V_{dd} is drawn to the grown through input and tail transistor. Thus, result in static power consumption.

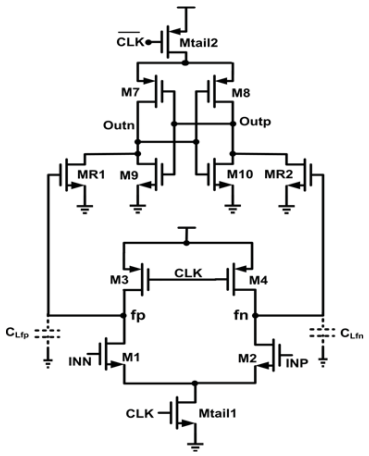

Figure 3. Schematic diagram of conventional double-tail comparator design

Result obtained by this comparator design exhibit power consumption about 12 µW and delay about 7.4 ns using 0.18 µm CMOS technology with VDD = 0.8 V.

II. DESIGN METHODOLOGY

Fig. 4 shows the flow chart for this project. There are several steps in designing the high speed comparator with low power consumption. Both design proposed and conventional double-tail comparator is design with 0.13 µm technology using Mentor Graphic tools.

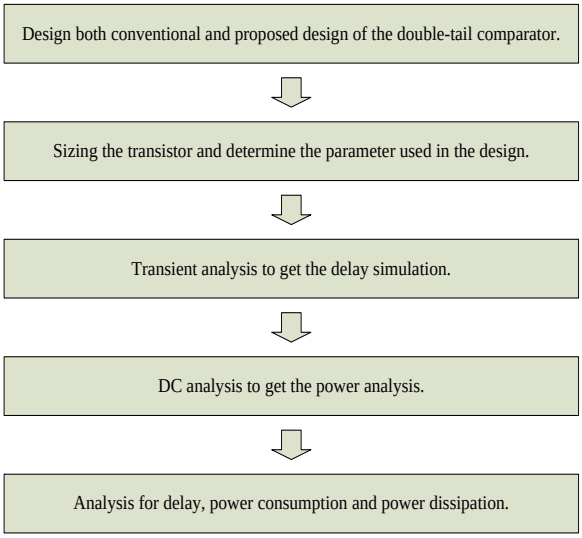

Figure 4. The flow chart of the design project

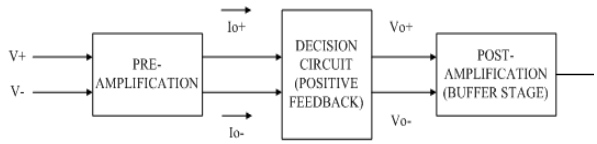

Figure 5. Block diagram of comparator

The comparator basically consists of three main stages. It is an input stage as the first stage. Next, the decision stage and also the last stage is the output stage. The input stage of the comparator normally will amplify the input signal. The decision stage is the main stage in the comparator that it is used to determine and choose which of the input signals is higher. The final stage is the output stage that is shown in Fig. 6. The main purpose of this final stage is that to convert the output of the decision making stage into a logic signal [8].

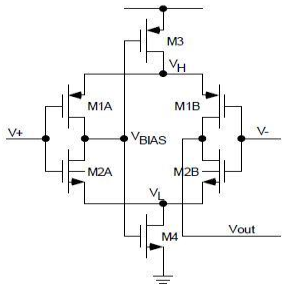

Figure 6. Schematic diagram of output buffer

In other to compare the performance in term of propagation delay, speed, power consumption and power dissipation of the double-tail comparator, both conventional and proposed double-tail comparator is designed. The circuit design for conventional and proposed comparator is shown in Fig. 3 and Fig. 7 respectively [9] [10].

a) Proposed Comparator design

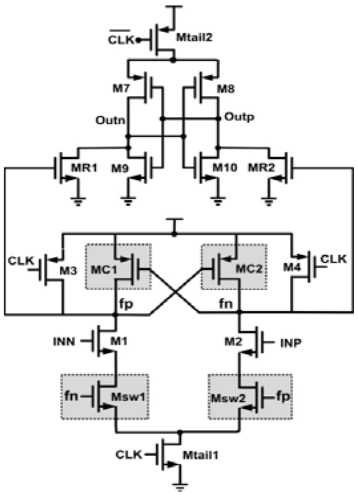

Figure 7. Schematic diagram of proposed double-tail comparator design

Fig. 7 demonstrates the schematic diagram of the proposed double-tail comparator. This design is modified from the previous comparator design which is based on conventional comparator structure. Because of the better performance of double-tail comparator architecture in low-voltage application, this proposed design followed [3]. The main idea of this proposed comparator is to increase $\Delta V\ f_n/f_p$ in order to increase the latch regeneration speed. For this purpose, two additional transistors (Mc1 and Mc2) that acts as control transistors is used and it is parallel to transistor M3/M4 but in a cross-couple manner. In this design, nMOS transistor (Msw1 and Msw2) as switches is used below the input transistor to overcome the static power consumption in the comparator design.

b) Operation of the Modified Comparator design

There are two phase for the operation of the proposed comparator design that can be described as follow. The first operation is that during reset phase (CLK = 0, *M*tail1 and *M*tail2 are off) this will avoid static power. While the transistor *M*3 and *M*4 are ON and pulls both fn and fp nodes to *V*DD, hence the transistor *M*c1 and *M*c2 are cut off. Intermediate stage transistors, *M*R1 and *M*R2 are ON which reset both latch outputs voltage to ground (0V).

The next operation is that during decision-making phase (CLK = *V*DD, *M*tail1, and *M*tail2 are on) and hence the transistors *M*3 and *M*4 turn off. At the beginning of this phase, the control transistors (Mc1 and Mc2) are still off since fn and fp are about

*V*DD. Thus, fn and fp start to drop with different rates according to the input voltages. Suppose *V*INP > *V*INN, thus fn drops faster than fp because transistor *M*2 provides more current than transistor *M*1. As long as fn continues falling, the corresponding pMOS control transistor which is transistor *M*c1 starts to turn on and it will pull fp node back to the *V*DD. So that for another control transistor *M*c2 remains off and allowing fn to be discharged completely. Therefore, the difference between fn and fp (*ΔV*fn/fp) increases [11] [13] [14].

There is one thing that should be considered in this proposed design is that, when one of the control transistors such as *M*c1 is turns on, a current from *V*DD is drawn to the ground via input transistor M1 and tail transistor Mtail1. It results in static power consumption. Thus, to overcome this issue, two nMOS switches (Msw1 and Msw2) are added below the input transistors.

Toward the start of the decision phase, both fn and fp nodes have been pre-charged to *V*DD (during the reset phase), both switches are closed (Msw1 and Msw2 ON) and fn and fp start to drop with different discharging rates. When the comparator detects that one of the fn or fp nodes is discharging faster, control transistors (Mc1 and Mc2) will act in a way to increase their voltage difference (*ΔV*fn/fp). Suppose that fp is pulling up to the *V*DD and fn should be discharged completely, hence the switch in the charging path of fp will be opened (Msw2 OFF) in order to prevent any current drawn from *V*DD but the other switch connected to fn will be closed (Msw1 ON) to allow the complete discharge of fn node.

III. RESULT AND DISCUSSION

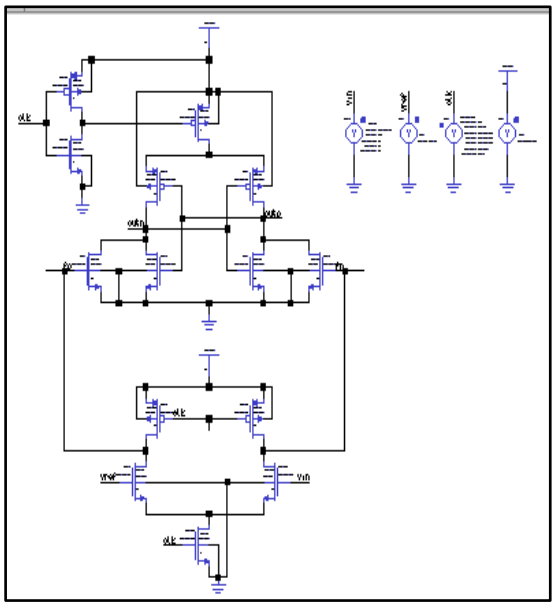

Figure 8. Schematic diagram of conventional double-tail comparator design in mentor graphics

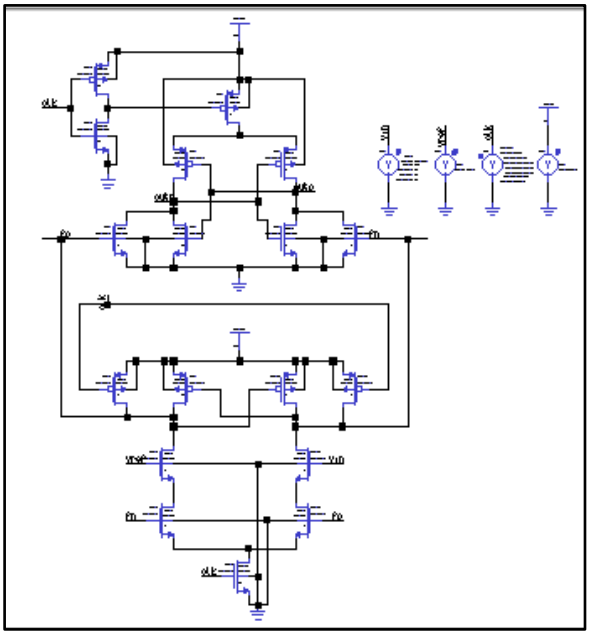

Figure 9. Schematic diagram of modified double-tail comparator design in mentor graphics

Fig. 8 and 9 shows the schematic diagram for conventional double-tail and proposed double-tail comparator design [15]. There are two inputs for both comparators that will be used in decision making phase. The two voltage inputs used in both design is the DC voltage and also sinusoidal voltage. The DC voltage is used as a reference voltage in these designs. The sinusoidal input voltage is set up with amplitude of 1 V and frequency of 800 MHz. There is pulse voltage in these designs and it acts as clock with a period of 3 ns.

The difference between these designs is that there are a number of additional transistors in the proposed design compared to conventional design. The purpose of additional transistors in the proposed design is that to overcome the static power consumption. Hence, the proposed design will have lower power consumption compared to the conventional design. Besides, the proposed design also results in the increasing speed when the schematic is design to increase the voltage difference at f_n and f_p nodes. The speed increases with the increasing voltage difference at that node.

A. Delay Analysis

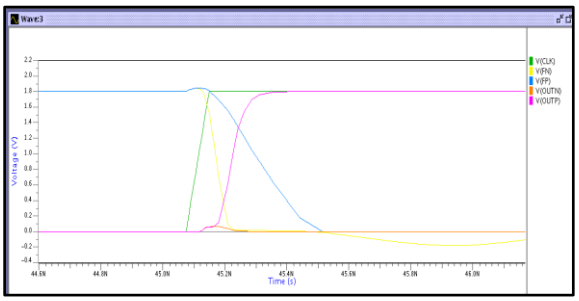

Figure 10. Transient simulation of the conventional double-tail comparator design

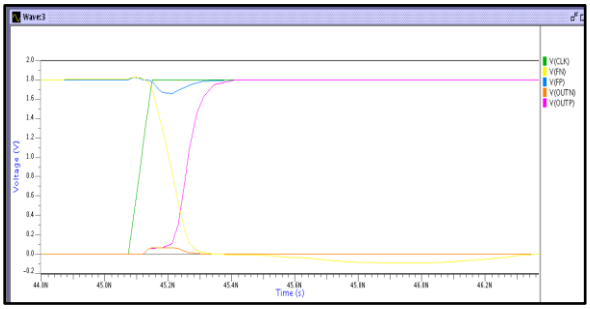

Figure 11. Transient simulation of the proposed double-tail comparator design

Fig. 10 and 11 shows the simulation results of the conventional and proposed design respectively. In the double-tail comparator design circuit, the propagation delay is calculated as in equation (1) [3] [16].

$$T_{PD} = T_0 + T_{LATCH} \quad (1)$$

Charge time T_0 is the time to charge the load capacitance of latch stage to turn on the latch regeneration. While latch delay T_{LATCH} is the time latch stage takes to give differential output half of the supply voltage V_{DD}.

$$T_0 = 2\frac{(V_{thn})(C_L)}{I_{LATCH}} \quad (2)$$

$$T_{LATCH} = \frac{(C_L)}{\text{gm,eff}} . ln\left(\frac{V_{DD}/_2}{\Delta V_0}\right) \quad (3)$$

So that, the propagation delays T_{PD},

$$T_{PD} = T_0 + T_{LATCH} \quad (4)$$

$$T_{PD} = 2\frac{(V_{thn})(C_L)}{I_{LATCH}} + \frac{(C_L)}{\text{gm,eff}} . ln\left(\frac{V_{DD}/_2}{\Delta V_0}\right) \quad (5)$$

B. Power Consumption

To determine the power consumption in both designs above, the total currents supply, Idd times with supply voltage, Vdd as shown in equation (6). The power consume, P of the comparator is proportional to the current, Idd and the supply voltage, Vdd [12].

$$P = I_{DD}V_{DD} \quad (6)$$

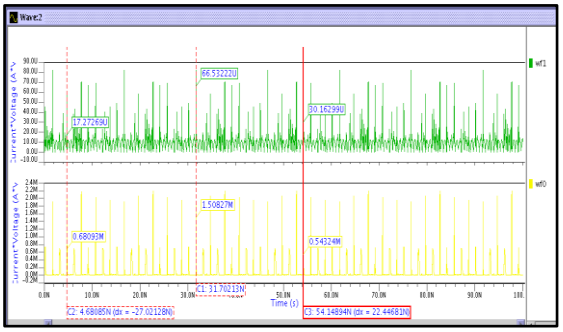

Figure 12. Power plot of the conventional (w0) and proposed double-tail comparator design (w1)

TABLE I. PERFORMANCE COMPARISON RESULT OF COMPARATOR

Performance characteristic	**Conventional Double-tail**	**Proposed Double-tail**
Supply voltage (V)	1.8	1.8
Power consumption (µW)	910.80	37.99
Power dissipation (nW)	14.17	14.29
Propagation delay (ps)	393.3	387.9
Speed (GHz)	2.54	2.58
Transistor count	14	18

Based on the table above, the result clearly shows that the proposed design gives lower power consumption compared to conventional design. Besides, the propagation delay of proposed design also gives lower value and means to higher speed of comparator. The power dissipation for proposed design is higher compared to conventional design. It is due to the additional transistors in the proposed design schematic.

IV. CONCLUSION

This paper has presented the design of two comparator circuits which are conventional and proposed double-tail design of comparator. The simulation results of both designs high speed and low power comparators are by considering 1.8 V power supply with frequency of 800 MHz. In this paper, the simulations have been done using Mentor Graphic Tools with Silterra 0.13 µm technology files. The comparison result has been done between the conventional and proposed double-tail comparator and the final result are shown in the Table I.

In conclusion, the proposed design shows the improvement in terms of propagation delay and also minimization of power consumption in the design. The reduction of propagation delay leads to higher speed of the comparator. At last, in the future recommendation these schematic can be design using small technology to achieve better performance of the devices.

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