Design and Analysis of a Fully Differential CMOS LNA for 3.1-10.6GHz UWB Communications Systems

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Abstract. ***An ultra-wideband (UWB) 3.1-10.6GHz low noise amplifier adopts cross-coupling commom-gate (CG) topology is presented in this paper. Inductive series-peaking is used for the LNA to obtain broadband flat gain in the whole 3.1-10.6GHz band. Designed in a commercial 0.18μm CMOS technology, the LNA achieves an NF of 3.1-4.7 dB, an S11 of less than -10dB, an S21 of 10.3dB and input 3rd interception point (IIP3) of -5.1dBm, while the power supply is 1.8V.***

Keywords: LNA, common gate, capacitive cross coupling, series peaking, UWB

I. INTRODUCTION

In 2002, the Federal Communication Commission (FCC) approved the operation of certain types of wireless devices incorporating the ultra-wideband (UWB) technology, which transmit information using very low power, short impulses thinly spreading over a bandwidth [1]. Low noise amplifier (LNAs) in UWB receivers must provide enough gain, low power consumption and low noise figure. UWB systems have recently received much attention because of their potential for high-speed wireless communication [2].

Most of the concern that surrounds the implementation of high-speed, UWB wireless technologies in a standard CMOS process is the analog front-end. The analog front-end in UWB wireless systems is one of the most crucial stages in determining overall system performance.

The amplifier must meet several requirements, such as input matching to minimize return loss, sufficient gain to suppress the noise, low noise figure (NF) to enhance receiver sensitivity and low power consumption to increase battery life.

There are several existing solutions for CMOS-based UWB LNA. The distributed amplifiers offer a wideband impedance match [3] but often have high power consumption due to need for multiple stages. The one stage common gate amplifier with local feedback (CGF) with inductive peaking provides good impedance matching performance [4], but it requires too much current for low power applications. The cascade LNA with inductive source degeneration provides good impedance matching and a low noise figure [5] but tends to suffer high IIP3. The distributed amplifiers (DA) provide good impedance matching, flat gain over a wide range of frequencies. However, the demand for high quality transmission lines makes them less attractive to low-cost application because of the larger area [6].

In this paper, the gm-boosted CG LNA concept is used in the fully differential capacitive cross-coupling CG LNA. The inductive series-peaking technique is using to achieve wideband flat gain. The expected of the proposed LNA achieves good input matching, low NF and high linearity [7].

II. CIRCUIT DESCRIPTIONS

A. Capacitive Cross Coupling CG LNA

The CG CMOS amplifier has an input impedance of 1/gm, where gm is the transconductance of the input resistor. Therefore, it is easily obtained by setting 1/gm to 50Ω. Hence, common-gate amplifiers can be more easily matched and usually exhibit better linearity than common-source. The capacitive cross-coupling has been used for gain enhancement and matching.

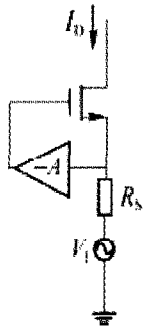
The derived noise factor expression of a CG LNA is:

$$F = 1 + \frac{\gamma}{\alpha gmRs} \qquad (1)$$

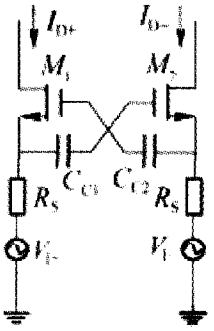
α and γ are biased-dependent noise parameter of MOS transistors and Rs is the source impedance.

From Eq. (1), the noise performance will be improved as the g_m is increased. However, this will deteriorate the input matching performance. The g_m-boosted concept is to decouple the noise performance from input matching in CG LNA which has an effective transconductance of $(1+A)$gm[8]. Its noise factor is reduced to:

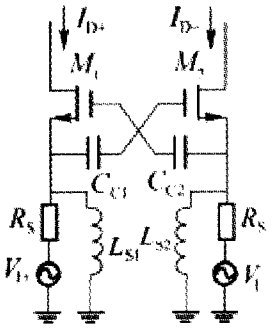
$$F = 1 + \frac{\gamma}{\alpha(1+A)^2} = 1 + \frac{\gamma}{\alpha(1+A)} \qquad (2)$$



a) Gm-boosted CG LNA



b) Capacitive cross-coupling CG LNA



c) Capacitive cross-coupling CG LNA for UWB

Figure 1: Schematic of CG LNAs

Rs is eliminated to increase differential gain [8]. The input matching of the gm-boosted CG LNA is implemented at a smaller bias current at the condition of $(1+A)g_mRs=1$. In Ref [6], the capacitive cross-coupling method is adopted to implement the inverting gain. The advantage of the capacitive cross-coupling CG LNA is that it is inherently suitable for fully differential operation.

The parasitic capacitance is taken into consideration, the input impedance is:

$$Z_{in}(s) \approx \frac{1}{(1+A)g_m + s2C_{gs}} \qquad (3)$$

From Eq. (3), the input matching performance will deteriorate at a high frequency because of the parasitic capacitance; Cgs. Cgs is the capacitance between the gate and source nodes of M1 and M2. To obtain good input matching at the desired UWB frequency band, a pair of inductors must be added at the input node to resonate with the parasitic capacitance. The resonance frequency is:

$$\omega_s \approx \frac{1}{\sqrt{C_{gs}\, L_{s1}}} \qquad (4)$$

The desired input matching performance can be obtained by adjusting Ls1 and Ls2 to locate ωs at the center of the 3.1-10.6GHz.

B. Series Peaking

Peaking technique are commonly used in enhancing the bandwidth of wideband amplifiers. The series peaking system in which the inductance is placed in series with the load capacitance. The gain of the amplifiers can be expressed as:

$$A(s) = \frac{V_{out}(s)}{V_{in}(s)} = g_m Z(s) \qquad (5)$$

where g_m represent the transconductance of M1, Z(s) denotes the transimpedance of the amplifiers. The bandwidth is dependent on Z(s) because g_m is approximately constant. Z(s) is denoted as:

$$= \frac{R_D}{1 + sR_D(C_1 + C_2) + s^2 L_D C_2 + s^3 L_D C_2 R_L C_1} \qquad (6)$$

Figure 2 shows the series-peaking amplifier.

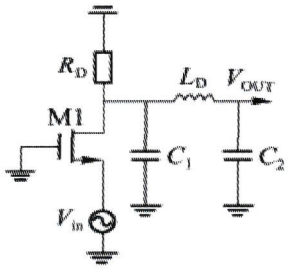


Figure 2: Series-peaking

III. CIRCUIT DESIGN

The schematic of fully differential LNA is shown in figure3[7]. The circuit consists of a capacitive-coupling CG LNA core with series-peaked loads. The input impedance matching is achieved by adjusting the size bias current of M1 and M2. Cascode transistors M3 and M4 are added to improve the reverse isolation of the LNA.

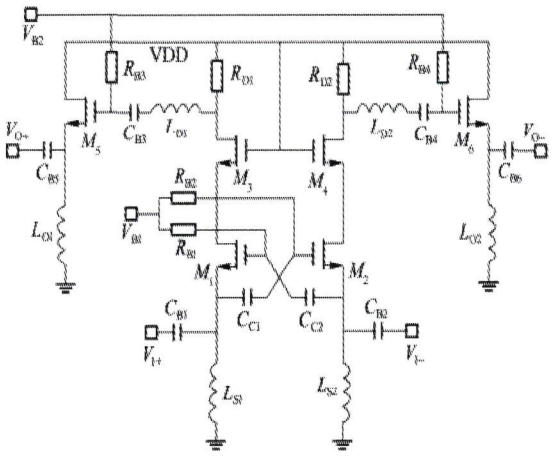
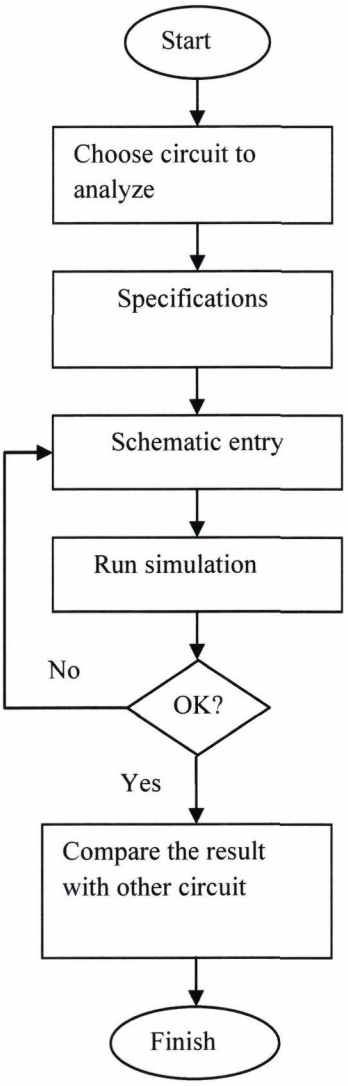


Figure 3: Schematic of the proposed LNA

TABLE 1: SUMMARY OF INSTANCE PARAMETER

Instance	Parameters	Instance	Parameters
M1, M2	W/L=100/0.18 μm	R_{D1}, R_{D2}	300 Ω
M3, M4	W/L=60/0.18 μm	C_{C1}, C_{C2}	10 pF
M5, M6	W/L=80/0.18 μm	R_{B1}~R_{B4}	3 kΩ
L_{S1}, L_{S2}	4.1 nH	C_{B1}~C_{B6}	5 pF
L_{D1}, L_{D2}	4.6 nH	L_{O1}, L_{O2}	3.6 nH

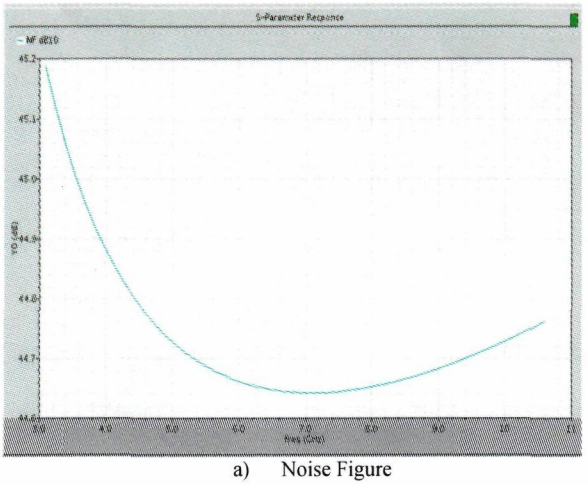
IV. METHODOLOGY



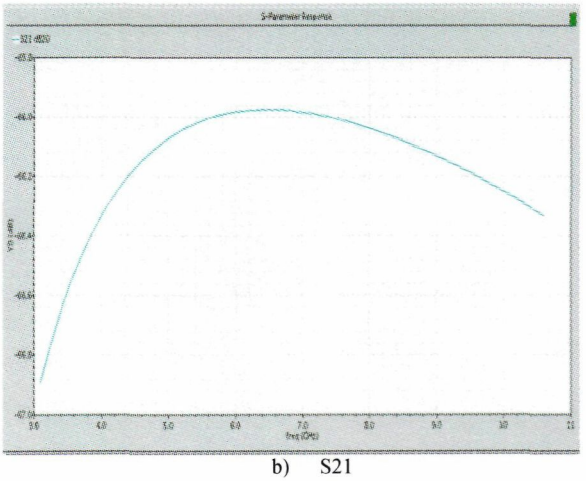
The basic design flow of an analog IC design, together with the CADENCE tools required in each step. First, the author has selected the circuit that suitable to analyze. Then, a schematic view of the circuit is created using the CADENCE Composer Schematic Editor. Alternatively, a text netlist input can be employed. Then the circuit is simulated using the CADENCE Affirma analog simulation environment. The author decide to analyze a fully differential CMOS LNA for 3.1-10.6GHz UWB communication systems. The parameter is going to be analyzed and look into the performance of the circuit after run simulation. The scope of this project is to simulate input return loss (S11), output return loss (S22), reverse isolation (S12) noise figure (NF) and 3rd interception point (IIP3). In completing this project, some research has been done in order to compare the result with other circuit. Thereafter, the author has been optimizing input return loss (S11) and noise figure (NF) due to varying L_s.

V. RESULT AND DISCUSSION

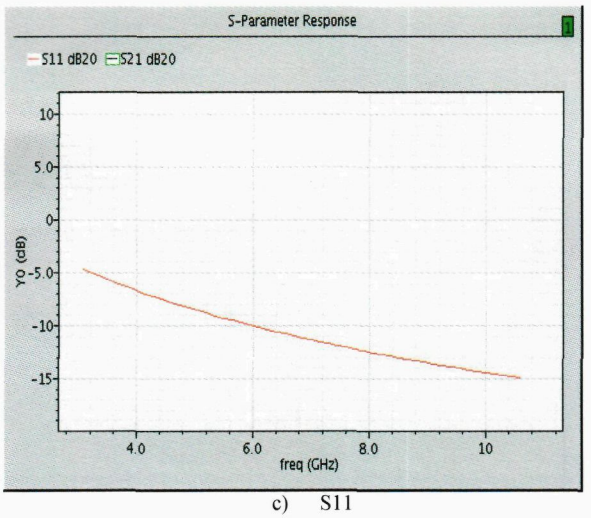
The simulated results are shown in figure 5. Two ideal baluns are used to obtain the performance of the fully differential LNA. The NF of the LNA is 44.62dB. The LNA achieves an S21 of -65.96dB, an S11 of below -10dB, an S12 of less than -50dB, and an S22 of less than -10dB. The IIP3 is -4.8dBm.



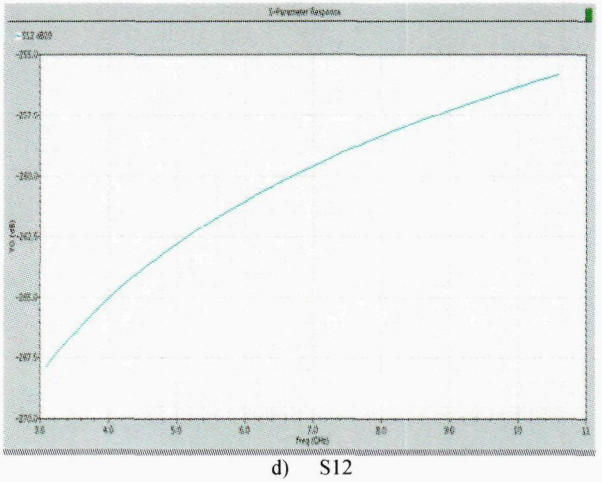
a) Noise Figure



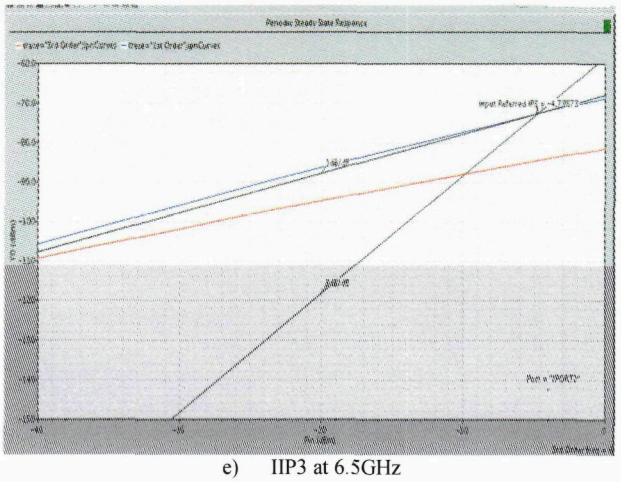
b) S21



c) S11



d) S12



e) IIP3 at 6.5GHz

Figure 5: Simulated performance of the LNA

Table 1 summarizes the performance of the proposed LNA, with comparison to some published CMOS LNAS.

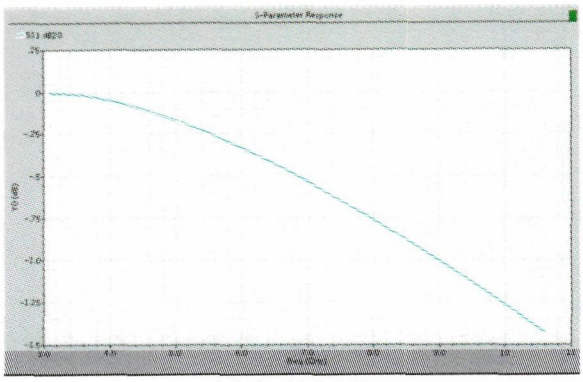
TABLE 2: PERFORMANCE SUMMARY AND COMPARISON

	[9]	[10]	[11]	Ref paper [7]	This work
NF/dB	4.5-5.1	4-8	4.5-5.1	3.1-4.7	44.64
S11/dB	<-11	<-9.9	<-11	<-10	<-10
S21/dB	11.5	9.3	9.7	10.7	-65.96
IIP3/dBm	+10	-6.7	-6.2	-5.1	-4.8

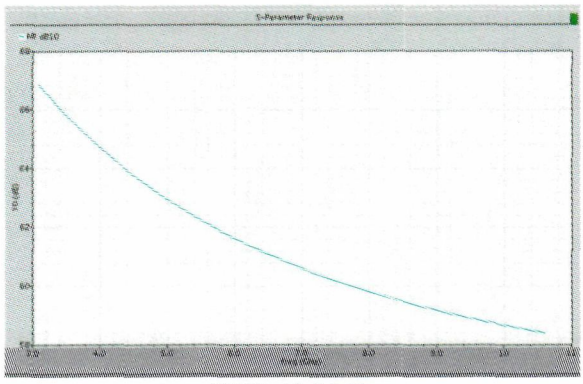
According to table 2, noise figure and S21 can't achieve as it will discussing in an introduction. The author had made some research about the result. Noise figure will degrade regarding the S-parameter. S-parameter depends on L_s. In addition to that, the testbench that is using during simulation, perhaps the baluns or the capacitor is not suitable for the circuit. On the other hand, the reference paper [7] had using post-layout simulation result. This paper had using schematic simulation result. Hence, the simulator may not include the layout effect. There will be electric and magnetic coupling around the circuit which may have a detrimental effect of the circuit.

A. Optimize Input Return loss (S11) And Noise Figure (NF)

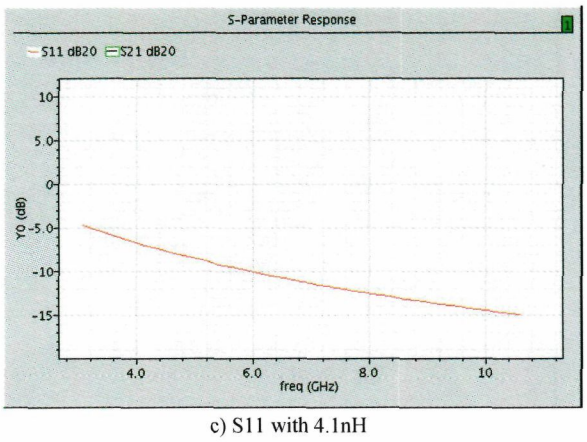
Hence, the author will vary L_s in order to optimize input return loss and noise figure. The author had chosen less or more value of L_s from the reference value. This is because, the author want to look at the performance when the L_s less or more. Simulated results are shown in figure 6.



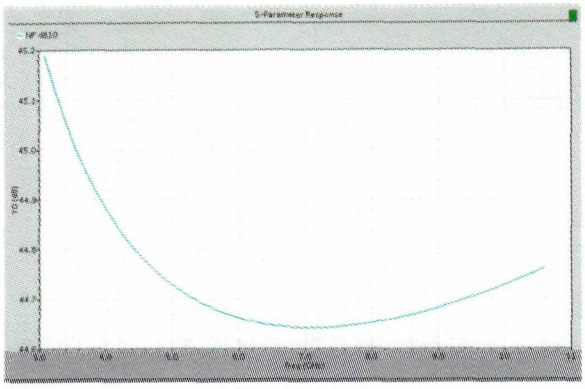
a) S11 with 0.5nH



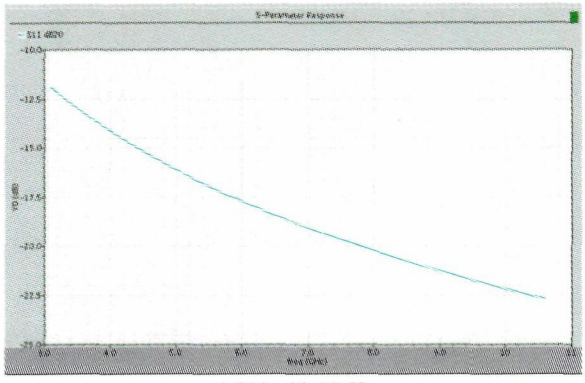
b) NF with 0.5nH



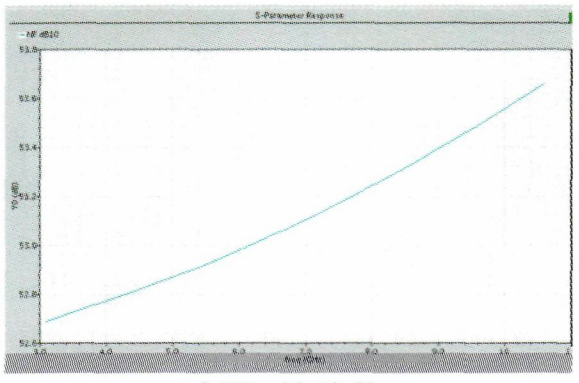
c) S11 with 4.1nH



d) NF with 4.1nH



e) S11 with 10nH



f) NF with 10nH

Fig. 6. Simulated performance of S11 and NF

Table 2 shows the result of the NF and S11 after done optimization.

TABLE 3: PERFORMANCE OF S11 AND NF

L_s	S11/dB	NF/dB
0.5nH	< -1.25	58.2
4.1nH (ref. value)	<-10	44.64
10nH	< -23	52.68

VI. CONCLUSIONS

This paper presents a fully differential CG LNA that adopts capacitive cross-coupling architecture for 3.1-10.6GHz UWB receivers. After done simulation, there are some of parameters are differ from the reference [7]. The different are regarding the different stages that is using during the simulation. In addition to that, the simulation in reference [7] is implemented with Spectre after layout design and parasitic extraction. However, this work is simulating after design schematic without considering the parasitic extraction.

Hence the author had make optimization of S11 and NF due to L_s. According to table 3, S11 will get less if the L_s had higher value. After make some research with other papers, the better performance for S11 is < -10dB.

On the other hand, if the L_s larger or smaller than the original value, the NF tends to suffer from high value.

ACKNOWLEDGMENT

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