Analysis of Pipeline ADC Performances with Different Sample and Hold Circuits

Asma Binti Mohd Salleh
Faculty of Electrical Engineering
University Teknologi MARA (UiTM)
Shah Alam, 40450, Selangor, Malaysia
asma_mohdsalleh@yahoo.com.my

***Abstract*—This paper present the analysis of pipeline analog-to-digital converter (ADC) with different architecture of sample and hold circuits. We focused on the comparison of the 1-bit pipeline ADC performances in term of speed and power using double buffer and double sampling sample and hold (S/H) architectures. S/H circuit is the most power hungry block that plays a crucial role in pipeline ADC. An appropriate and precise S//H circuit is needed in order to optimize the power dissipation of pipeline ADC without affecting its performances. This pipeline ADC was designed and implemented using CMOS 0.18µm technology with 1.8V supply voltage in Silvaco EDA tool. Double sampling S/H is suitable for pipeline ADC since it consume less power and faster than double buffer S/H at low clock period.**

Keywords-analog digital converter; double buffer sample and hold; double samplings sample and hold.

I. INTRODUCTION

The basic function of analog-to-digital converter (ADC) is to convert the analog signal to digital signal. Most of the signal in real world is an analog signal thus these signals need to be converted into digital signals so that it can be read, understand and manipulated by microprocessor.

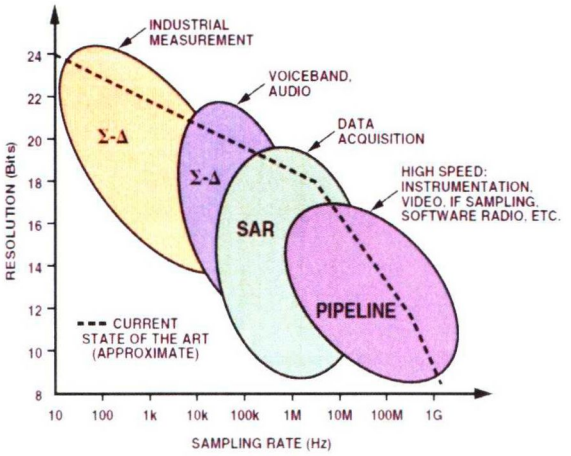

Figure 1. ADC architectures, applications, resolution, and sampling rates cited from [7].

There are several types of ADC such as Flash ADC, Successive-approximation-register (SAR) ADC, Sigma Delta ADC and pipeline ADC. Selecting the proper ADC should be done by considering the particular application. Based on Fig. 1 pipeline ADC has the highest sampling rate than the other ADC architectures but has the weakness in term of smallest resolution between 8 to 16 bits. Thus, pipeline ADC is suitable for high speed applications including data communication and image signal processing [8].

The increase importance of ADC has driven the demand for low power and high speed ADC. The requirement of high speed, low distortion and low noise in processing of analog signal often translate into poor power efficiency and limited throughput [1]. Pipeline ADC faced with a subtle issue relating to most CMOS pipelined ADCs performance at low sampling rates. The low sampling rates will cause the extension of the hold times where excessive droop can cause errors in data conversion [7].

By considering the signal converting operation, S/H circuit is the most important block in pipeline ADC because the sampling frequency for S/H circuit is represents the speed of the converter. Typically the S/H circuit in a pipeline ADC is the most power-hungry block due to its high performance requirement [2]. Thus, an appropriate S/H circuit is needed to implement the pipeline ADC in order to optimize its power while maintaining its speed.

Most of pipelined ADCs include a sample-and-hold (S/H) circuit at the front-end because the performance of S/H circuit is critical to the overall ADC dynamic performance [2].

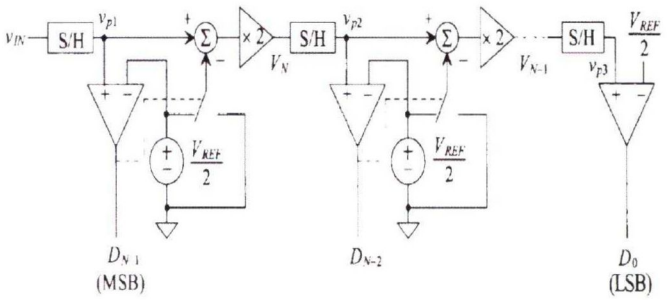

Figure 2. Block diagram of a pipeline ADC cited from [3].

Fig. 2 is the block diagram of a pipeline ADC. It consists the block of S/H, comparator, adder, gain 2 amplifier and switch. The output of comparator is the digital output of n-bit and the

output of gain 2 amplifier will become the input signal of next state of pipeline ADC.

This paper present the comparison of 1 bit pipeline ADC in term of its speed and power using two different block of S/H, which is double buffer and double sampling sample and hold (S/H).

A. Double buffer S/H architecture

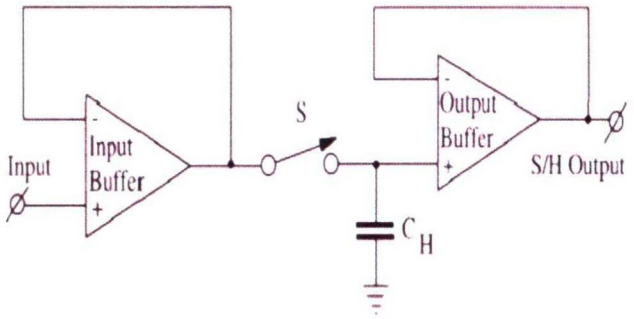

Figure 3. Double buffer S/H circuit cited from [11].

Fig. 3 is the circuit of double buffer S/H architecture that consists of two buffers, a switch and a capacitor.

During sample mode the switch is closed and the voltage on the capacitor tracks the input signal. While during the hold mode switch is opened and the input voltage level at the opening switch will be held by capacitor [9].

The stability of this architecture determine by the stability of the op-amp. If the op-amp offset used to implement this block is large, then the accuracy of this block will be affected [11].

B. Double sampling S/H architecture

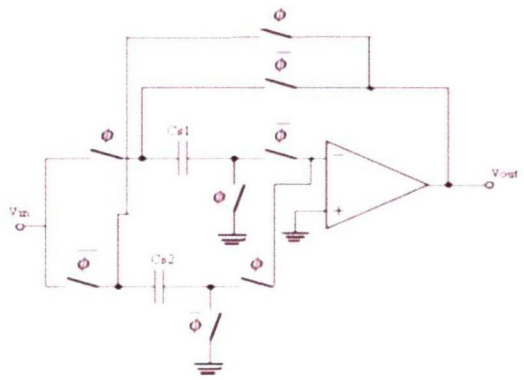

Figure 4. Doubled sampled sample and hold circuit cited from [9]

Fig. 4 is the circuit of double sampling S/H architecture. This architecture consists of an op-amp, 2 capacitors, and 8 switches. It has two parallel sampling circuits that controlled by opposite clock phase.

This architecture provide twice sampling rate and also suitable for high speed application but may result in timing mismatch between these two signal [9].

II. METHODOLOGY

A. Flow chart

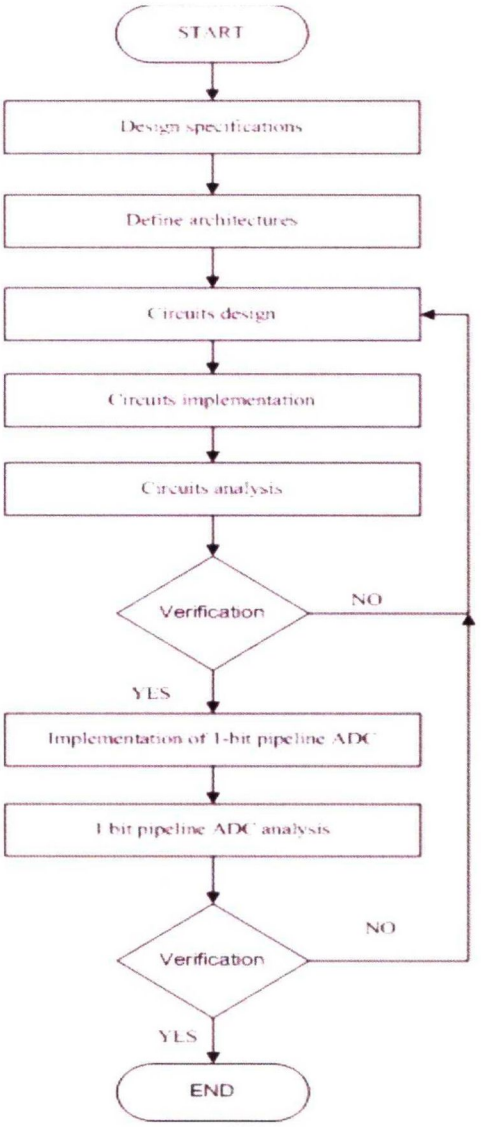

Figure 5. Project design flow chart

Based on Fig. 5, the project design flow starts with the design specifications of pipeline ADC. This pipeline ADC has supply voltage 0f 1.8V that implemented using 0.18um technology and produce 1 bit output. In defining the architecture, the double sampling and double buffer S/H circuits was used while the other blocks are the same for both complete pipeline ADCs. For circuit design stage, the ratio of pmos to nmos was 3.5. This ratio was chose based on the inverter voltage transfer curve. Each block was implemented in Silvaco EDA tool and the analysis was done whether in ac, dc or transient in order to verify the behavior of these blocks. After the verification was completed, each block was combined to make a complete system of a pipeline ADC. The complete system of pipeline ADC was simulated in order to verify its behavior. If the complete system is fail, the flow will be start again at designing the circuit.

B. 1 bit pipeline ADC

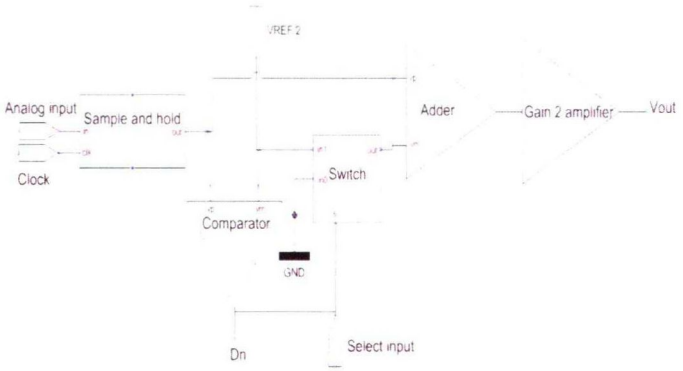

Figure 6. Schematic 1 bit pipeline ADC

Fig. 6 shows the schematic of 1 bit pipeline ADC that comprises of S/H, comparator, switch, adder, and gain 2 amplifier block. 1-bit pipeline ADC receives clock, analog signal and Vref/2 as its inputs and produces one digital bit (Dn) and output voltage (Vout). Dn is the digital bit of the current state and Vout of the current state will be the input of S/H of the next state. Since, only 1-bit pipeline ADC was implemented, Vout is not connected to anything. The S/H block received the analog signal and clock pulse as its inputs. The output of S/H sent to the positive input (Vp) of comparator and Vp of the adder. The S/H block will waiting for the clock in order to perform sample at positive clock edge then it will hold that value until the next positive clock edge.

The comparator receives its input from the output of S/H and compares it with value Vref/2. In this case, the value of Vref/2 is 0.9V. If the output of S/H is larger than 0.9V, then the output comparator is one and if not, the output of comparator is zero. Then, the switch will receive its input from Vref/2 and the other input of switch is zero. Dn will be the select input of the switch that will choose zero or Vref/2. The output of switch depends on the value of Dn. If Dn zero, output switch is zero, if Dn is 1.8V the output of switch is 0.9V. Then this ADC will perform subtraction of the output of S/H to the output of switch and amplify the held signal by 2.

i. S/H block

a. Double buffer S/H

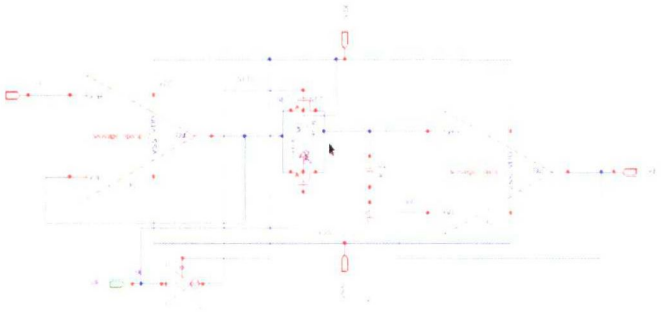

Figure 7. Schematic double buffer ADC

Fig. 7 is the schematic of double buffer S/H that used 1pF of hold capacitor. A transmission gate was used as switch, which was controlled by the clock. When clock is high, the switch will be on and the output is equal to the input voltage while at the same time the capacitor is charging to the potential of input voltage. As the clock change from high to low, the switch will be turn off and the output potential will be same as the potential hold by capacitor.

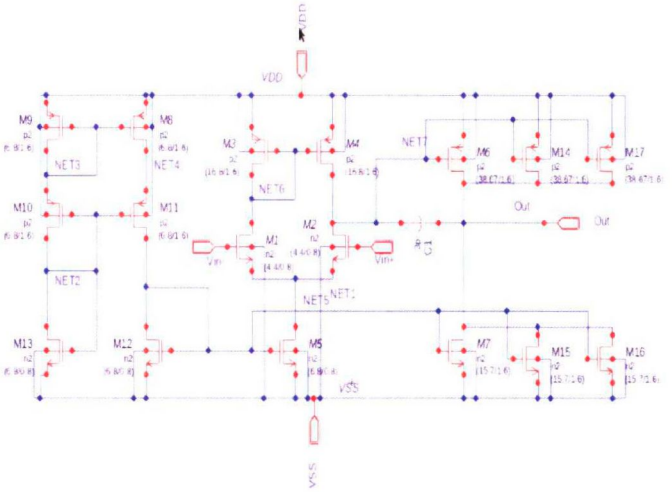

Figure 8. Schematic Two stage op-amp

Fig. 8 is the schematic of two stage op-amp that was used inside the double buffer S/H block and others block except comparator and switch blocks. The first stage of op-amp is a differential amplifier that converts the differential input voltages to differential currents. These differential currents are sending to the current-mirror load and become the input voltage for the second stage of op-amp. The second stage will convert the second stage input voltage to current and pass to the current sink load in order to convert the current to voltage at the output [13].

b. Double sampling S/H

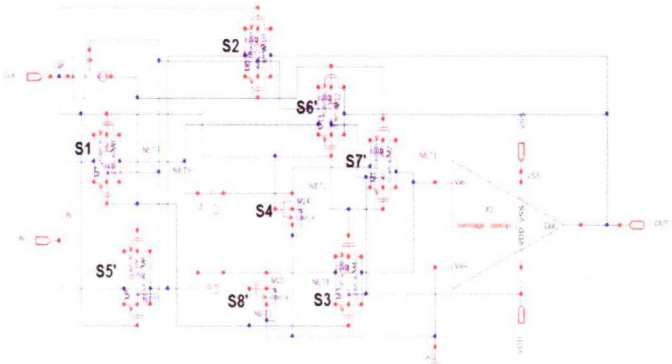

Figure 9. Schematic double buffer ADC

Fig. 9 is the schematic of double sampled S/H consists of an op-amp, two capacitors, 8 switches and an inverter. Again, the inverter was used to control the gate of transistors of switches. Switches S5 to S8 have opposite clock than the clock phase of switches S1'- S4'. During sample mode, switches S1 to S4 are turn on. Switch S4' and S8' were implemented use single pmos since they were used to make connection to ground and pmos can pass zero perfectly.

ii. Switch

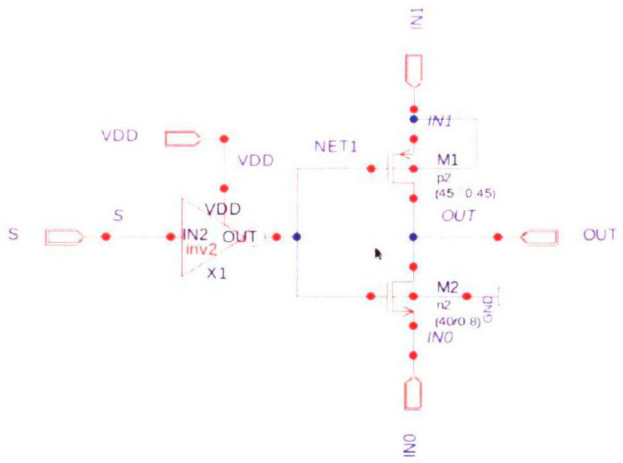

Figure 10. Schemtic of switch

Fig. 10 is a switch consists of an inverter and two transistors. The inverter was used to turn on these transistors. This switch is actually has same operation as 2-to-muxtiplexer that has one select input(S). In this clock, S is connected to the inverter so that it turn nmos or pmos transistor.

If select input (S) is low, the first transistor, M1 turns on and passes the first input to the output, but if S is high, the second transistor, M2 turns on and passes the second input to the output.

iii. Adder

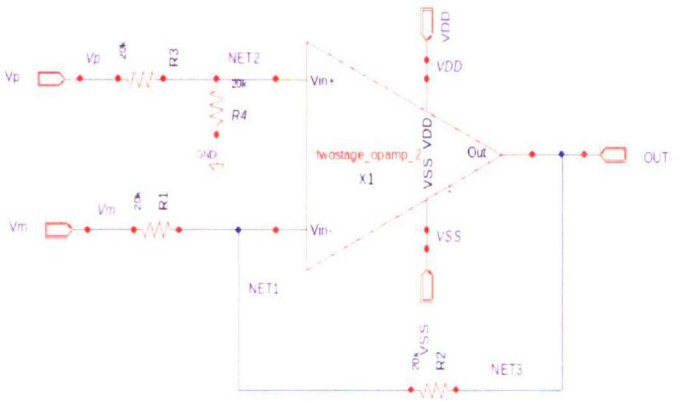

Figure 11. Schematic of adder

Although a pipeline ADC consists of an analog adder as described in [3], actually this block was performing a subtraction operation. In this paper, the analog adder was implemented using a two stage op-amp and four resistors. The output of this block in Fig. 11 can be written as

$$Vout = -Vm(R2/R1) + Vp(R4/R3 + R4)(R1 + R2/R1) \quad (1)$$

If R1 = R2 = R3 = R4, then equation (1) can be written as

$$Vout = Vp - Vm \quad (2)$$

iv. Gain 2 amplifier

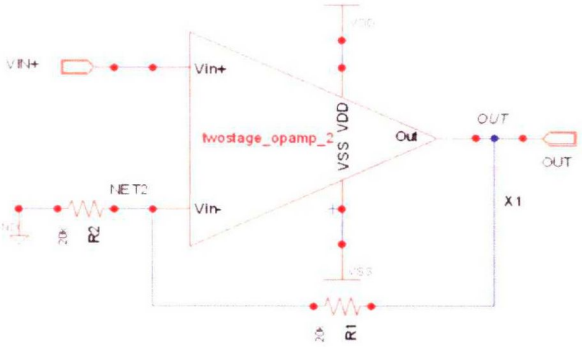

Figure 12. Gain 2 amplifier

The gain 2 amplifier in Fig. 2 was implemented using a two stage op-amp and two resistors. This block will multiply the output of analog adder by 2. Its output can be written as

$$Vout/Vp = 1 + R1/R2 \quad (3)$$

If R1 = R2, then equation (3) can be written as

$$Vout/Vp = 2 \quad (4)$$

III. Result and Discussion V/us

i. Two stage op-amp

TABLE I. TWO STAGE OPAMP SIMULATION RESULT

Parameter	Specifications
Gain	70.47 dB
Gain bandwidth	2.46 MHz
Positive slew rate	0.96 V/us
Negative slew rate	-0.87 V/us
ICMR	-0.7V – 1.7V
CMRR	69.32 dB
Output swing	-1.79V – 1.79V
PSRR+	74.58 db
PSRR-	73.87 db
Power consumption	25.2uW

From Table I, the op-amp gain is 70.47 dB. The higher the gain is better because small gain can cause the degradation of its output. The simulation show that the two stage op-amp has gain bandwidth of 2.46 MHz. Larger gain bandwidth requires large power consumption [14], thus the op-amp gain bandwidth must be reduced in order to optimize the power. The slew rate can be defined as the rate of changed of output voltage. The distortion of signal will happen if the op-amp slew rate is too large. The other important op-amp characteristic is Input Common Mode Range (ICMR). The

range of the designed op-amp in this paper is from -0.7V to 1.7V. The input voltage must not exceed this range so that it will not affect the performances of ADC.

ii. Analog adder

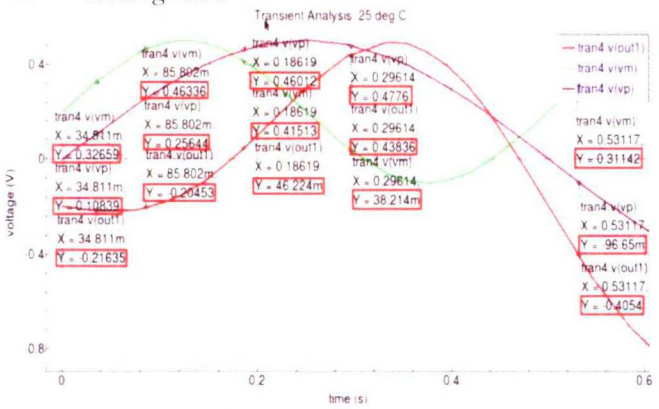

Figure 13. Analog adder transient analysis

TABLE II. ANALOG ADDER TRANSIENT ANALYSIS

Input		Output	%Error
Vp	*Vm*		
0.10839	0.32659	-0.21635	0.85
0.25644	0.46336	-0.20453	1.16
0.46012	0.41513	0.04622	2.73
0.47760	0.43836	0.03821	2.62
-0.09665	0.31142	-0.40540	0.65

$$\%\,\text{Error} = \left|\frac{\text{Measured- Actual}}{\text{Actual}}\right| \times 100 \qquad (5)$$

Fig. 13 showed the transient analysis of analog adder.The analog adder circuit was simulated using two sine inputs. Five random points was measured and shown in the Table II.

Equation (5) is the formula that has been used to calculate the percentage of error. As the input of adder increase, its percentage of error is also increase.

iii. Gain 2 amplifier

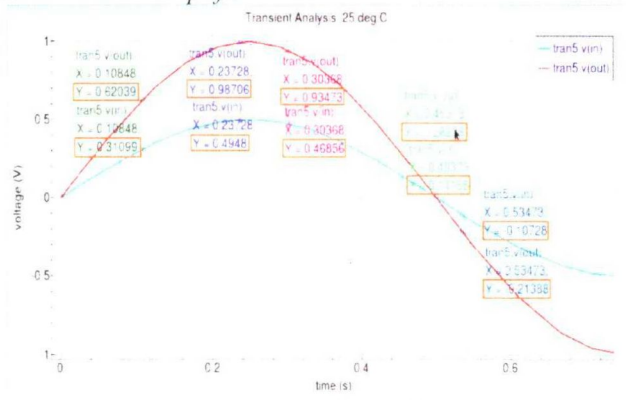

Figure 14. Gain 2 amplifier ac analysis

TABLE III. GAIN 2 AMPLIFIER AC ANALYSIS

Input (Vp)	Output	%Error
0.31099	0.62039	0.26
0.49480	0.98706	0.26
0.46856	0.93473	0.26
0.14155	0.28238	0.25
-0.10728	-0.21388	0.32

The gain 2 amplifier was simulated using a sine wave as input with amplitude of 0.5 and five random points was measured and show in Table III. The percentage of error is about 0.26 but it increase as input decrease.

The errors of adder and gain block are cause by the non-ideal parameter of the designed two stage op-amp. These errors can be reducing by using high performances of op-amp.

iv. Switch

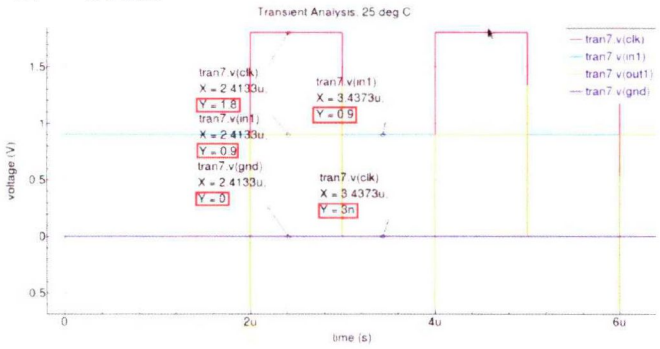

Figure 15. Switch transient analysis

TABLE IV. SWITCH TRANSIENT ANALYSIS

Input			Output	%Error
IN0	*IN1*	*S*		
0	0.9	0	3n	0
0	0.9	1.8	0.9	0

If the select input (S) is low, the output will be same as the first input (IN0), and if the S is high the output will be same as second input (IN1). From the simulation in Table IV, when select input is 0, the output is 3n and if the select input is 1.8V, the output is 0.9V. The result is almost same with the theoretical value with percentage of error approximately to 0.

v. Comparator

The comparator will compare its two inputs. If Vp>Vm, the the output of comparator is equal to VDD and if Vp<Vm, the output of comparator is 0. Based on Fig. 16, the comparator takes 2.29 ms to change its output from zero to VDD. Beside the S/H block, comparator also plays an important role in pipeline ADC. The longer the time taken of comparator to change its input to output can cause the pipeline ADC produce wrong digital output.

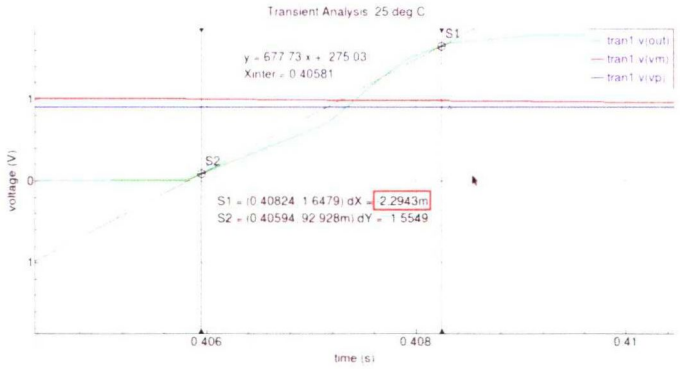

Figure 16. The positive edge of the output comparator

v. *Sample and Hold*

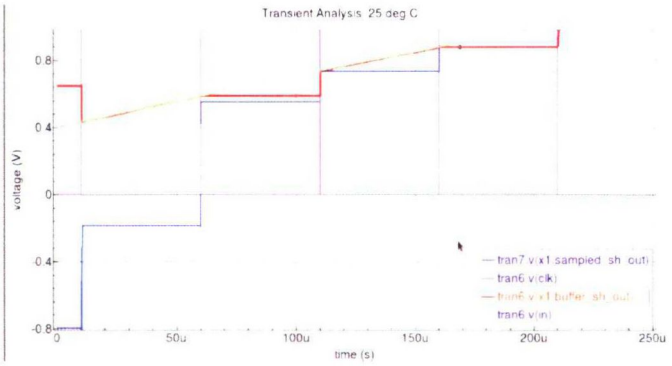

Figure 17. Double buffer S/H and double sampling S/H transient analysis at clock period of 0.1m

From Fig. 17, at 0.1m clock period the performance of double buffer S/H is accurate than double sampling S/H. On the first and second clock edge, the value hold by double sampling S/H is not same as the analog input. Only at the third clock edge, the output of double sampling S/H start to hold the exact value of input voltage.

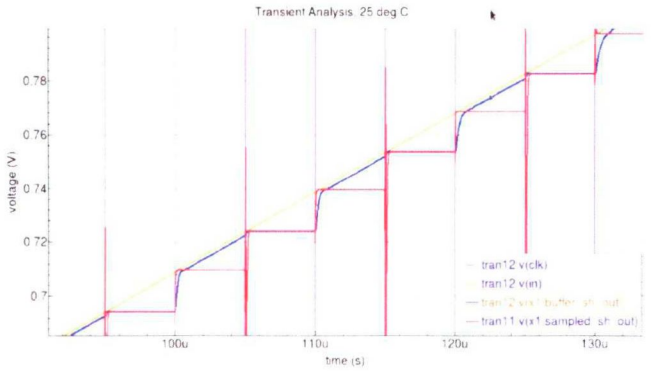

Figure 18. Double sampling S/H and double sampling S/H transient analysis at clock period of 0.01m

From Fig. 18, the performances of double buffer S/H start to degrade. Its output has become inaccurate as the input voltage, but the output of double sampling S/H maintain holding the value of input voltage. From Fig. 17 and Fig. 18, the double buffer S/H performs great performance at low speed, but its performances degrade at high speed.

vi. *1 bit pipeline Pipeline ADC*

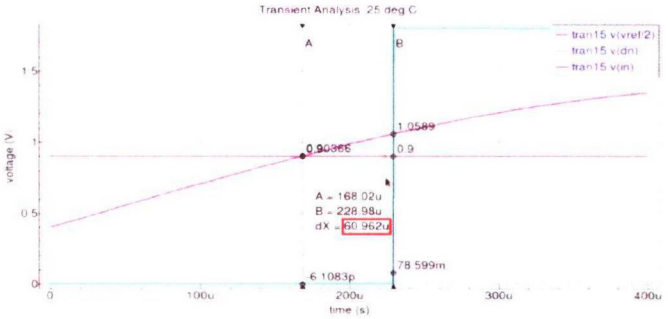

Figure 19. Different between analog input to digital output of 1 bit pipeline ADC with double buffer S/H architecture with clock period 0.1m

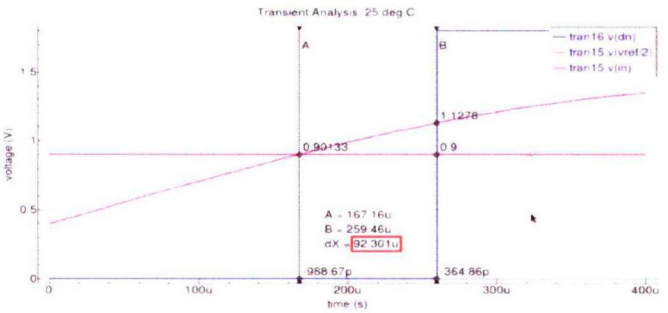

Figure 20. Different between analog input to digital output of 1 bit pipeline ADC with double sampling S/H architecture with clock period 0.1m

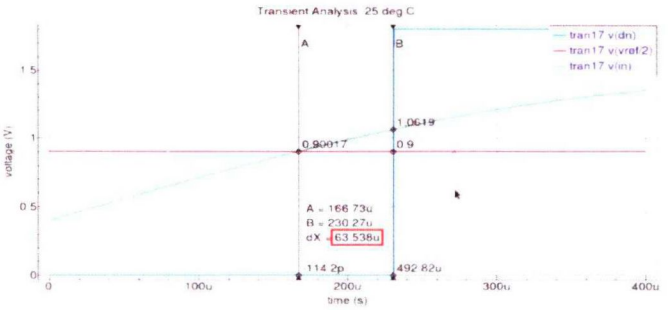

Figure 21. Different between analog input to digital output of 1 bit pipeline ADC with double buffer S/H architecture with clock period 0.01m

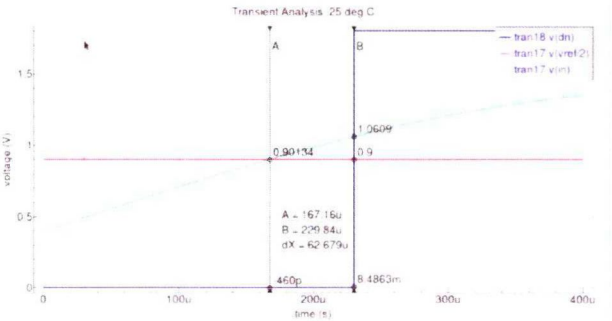

Figure 22. Different between analog input to digital output of 1 bit pipeline ADC with double sampling S/H architecture with clock period 0.01m

TABLE V. CONVERSION TIME OF 1 BIT PIPELINE ADC WITH DIFFERENT S/H ARCHITECTURE

	Conversion time (us)	
Clock period(ms)	*0.1*	*0.01*
Double buffer S/H	60.962	63.538
Double sampled S/H	92.301	62.679

From the simulation result in Table V, when clock period is 0.1ms the time taken of conversion analog to digital signal of pipeline ADC with double buffer S/H is faster than pipeline ADC with double sampling S/H. However, when clock period is 0.01ms the time taken of conversion analog to digital signal of pipeline ADC with double buffer S/H is slower than pipeline ADC with double sampling S/H. This result is affected by the block of comparator, although smaller clock period have been used, but it need to wait for comparator to perform the conversion. At large clock period, the pipeline ADC with double buffer S/H was faster but at small clock period, the pipeline ADC with double sampling S/H was faster.

TABLE VI. POWER CONSUMPTION OF 1 BIT PIPELINE ADC WITH DIFFERENT S/H ARCHITECTURE

S/h architecture	**Conversion time**
Double buffer	1.596mW
Double sampled	1.242mW

Power dissipation in ADC arises by the charging and discharging parasitic capacitance, short circuit current, leakage current and also dynamic power [15].

Based on the simulation in Table VI, the power consumption of double buffer is larger than double sampled S/H. The double buffer S/H architecture has larger number of transistor than the double sampled S/H architecture because it used two op-amps in its block. The increasing number of transistors causes the increasing power dissipation.

IV. CONCLUSION

The performances of pipeline ADC are highly affected by the performances of S/H circuit. The S/H circuit is the main component in the pipeline ADC that plays a crucial role in converting the analog to digital signal.

At high clock period, 1 bit pipeline ADC with double buffer S/H has faster conversion time of analog to digital signal and also has better performance in term of accuracy. While the 1 bit pipeline ADC with double sampling S/H has slower conversion time of analog to digital signal.

At low clock period, 1 bit pipeline ADC with double sampling S/H has faster conversion time of analog to digital signal and also has better performance in term of accuracy. While the 1 bit pipeline ADC with double buffer S/H has slower conversion time of analog to digital signal.

1 bit pipeline ADC with double buffer S/H consumes large power than 1 bit pipeline ADC with double sampling S/H. Thus, double sampling S/H architecture is suitable for pipeline ADC, since this ADC was used for high speed instruments.

For the future recommendation, since double sampling S/H circuits is faster and consume less power dissipation, it is suitable for pipeline ADC, but a precise implementation is needed in order to avoid the mismatch between its two parallel circuits.

REFERENCES

[1] Jay Shri Chouksey and Seema Kanathe, "Design and Implementation of 7-bit Pipeline Analog to Digital Converter," 2012 IEEE Fourth International Conference on Computational Intelligent and Communication Networks, pp 458-462, 2012

[2] Shan Jiang, Manh Anh Do and Kiat Seng Yeo, "A 200-MHz CMOS Mixed-Mode Sample-and-Hold Circuit for Pipelined ASCs," 2006

[3] R. Jacob Baker, CMOS Circuit Design, Layout and Simulation, revised 2nd ed., Wiley: United State of America, IEEE, 2008

[4] Alireza Abolhasani, Mohammad Tohidi, Khayrollah Hadidi and Abdullah Khoei, "A New High-Resolution and High-Speed Open-Loop CMOS Sample and Hold Circuit," IEEE, 2013

[5] Mohammad Hasan-Sagha and Mohsen Jalali, "Very High Speed and Low Voltage Open-Loop Dual Edge Triggered Sample and Hold Circuit in 0.18um CMOS Technology," IEEE-ICSE2012 Proc., 2012, Kuala Lumpur, Malaysia, pp 645-648, 2012

[6] Marcell Veloso Campos, André Luís Fortunato and Carlos Alberto dos Reis Filho, "New 12-bit Source-Follower Track-and-Hold Circuit Suitable for High-Speed Applications," 2011 IEEE/IFIP 19th International Conference on VLSI and System-on-Chip, pp 82-85, 2011

[7] Walt Kester, "Which ADC Architecture Is Right for Your Application?," 2005

[8] Mingjun Fan, Tingqian Chen, Wenjing Yin, Lei Wang, Ning Li and Junyan Ren, "A 8-bit 125-MSample/s Pipelined ADC," 2012

[9] YSunil Gavaskar Reddy, Andhrapradesh and Siek Liter, "A 1.2V 80Ms/s Sample and Hold for ADC Applications,"

[10] Ming-Jer Chen, Yen-Bin Gu, Jen-Yin Huang, Wei-Chen Shen, Terry Wu, and Po-Chin Hsu, "A Compact High-Speed Miller-Capacitance-Based Sample-and-Hold Circuit", IEEE, 1998

[11] Insoo Kim, Kyusun Choi, "Sample & Hold Circuits", unpublished.

[12] David Johns and Ken Martin, "Sample-and-Holds", unpublished.

[13] Allen, Phillip E., and Douglas R. Holberg, CMOS Analog Circuit Design. 2nd ed. New York: Oxford University Press, 2003.

[14] Imran Ahmed. Pipelined ADC Design and Enhancement Techniques. USA : Springer Heidelberg, 2010.

[15] R. M. Shende, P. R. Gumble, "Architecture of 4-bit Pipeline ADC In CMOS Technology", International Journal of Advanced Research in Computer Engineering & Technology, Volume 2, Issue 3, 2013