Performance Analysis of a Wideband LNA Utilizing 0.18µm Technology with HBM ESD protection

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Abstract-This paper presents the performance analysis of wideband low noise amplifier (LNA) design circuits utilizing 0.18µm CMOS technology. The objective of this performed analysis of a LNA design that need achieve sufficiently large gain and low noise figure, compare the design with other design, and to verify the effect of parameter R_f and L_s to S-parameter. This LNA design was expected to achieve a peak power gain of 13.8 dB. Within the 3 dB bandwidth from 2.6 GHz to 6.6 GHz, the noise figure (NF) is in a range of 4.0 dB to 6.5 dB and the input reflection coefficient, S_{11} is below -13.0dB.The standard specification for LNA with bandwidth from 2.6GHz is ISDB. This usually used for digital audio and video broadcasting application. By using Cadence Virtuoso as an EDA tool as a simulation tool, the result are obtained. The simulation result had almost achieved the target and this analysis had performed successfully simulation.

Index Terms—CMOS, Electrostatic discharge (ESD), low noise amplifier (LNA), wideband.

I. INTRODUCTION

Low-noise amplifier (LNA) is an electronic amplifier used to amplify very weak signals. LNA is the simple block in receiver most front ends .Using an LNA, the effect of noise from subsequent stages of the receive chain is reduced by the gain of the LNA, while the noise of the LNA itself is injected directly into the received signal. LNA is a part that amplifying the signal plus bring a minimal amount of noise to the signal.

Wideband is a term usually used in communication to describe a wide range of frequencies in a spectrum. A wideband amplifier is an electronic circuit providing constant amplification with a ratio of its low corner frequency to its high corner frequency of more than an octave.

The human body model (HBM) is the most commonly used model for characterizing the susceptibility of an electronic device to damage from electrostatic discharge (ESD). The model is a simulation of the discharge which might occur when a human touches an electronic device. In general, a tradeoff exists between the parasitic capacitance and ESD level. This effect becomes more critical for RF front-end circuits, which could seriously degrade the input reflection coefficient, gain, bandwidth, and also noise characteristic. [3]For RFIC design, the ESD protection circuit can no longer be treated separately. Instead, it must be considered simultaneously with other blocks for achieving best overall performance. [4]

The primary objective is to perform analysis of the LNA design that need to achieve sufficiently large gain and low noise figure to suppress the additive noise at the subsequent stages. The LNA circuit with HBM ESD needs to achieve the requirement as within the 3 dB bandwidth from 2.6 GHz to 6.6 GHz, the noise figure (NF) is in a range of 4.0 dB to 6.5 dB and the input reflection coefficient, S_{11} is below -13.0dB. Other than that, this paper also focused on the effect of parameter value, R_f and L_s to the S-parameter and Noise Figure and the comparison between other LNA design.

Different technique were proposed for the wideband RF LNA design, and less work that including ESD protection [5]-[9].In this study, a wideband LNA with a high level of ESD protection was proposed using 0.18µm MOS transistors.

II. LITERATURE REVIEW

A. LNA Configuration

There is several type of LNA topologies can be chose to design the LNA. Each of them will give different effect to the circuit performance. Some examples of the basic topologies are shunt input termination, shunt-series feedback amplifier, common gate amplifier; sources degraded common source amplifier and other.

For shunt input termination, the input matching adds more than 6dB noises to the Noise Figure (NF) whiles for common gate figure minimum value for NF but the transistor channel are in input signal.

In this paper, the cascade amplifier with a RC shunt-shunt feedback was proposed. The advantage of this topology are the gain sensitivity will reduces, overall gain become steady and widening of bandwidth of amplifier. Single ended topologies with cascade transistor are use for LNA implementation. The benefit of use this type of topology because cascade transistor helps to increase output gain and helps to reduce S21.Futhermore, output inductor resonates with output load will maximize output power transfer and gain at resonance frequency. The value of NF will also reduce.

B. LNA Parameter

In LNA design, Scattering parameter (S-parameter) and noise figure are the important parameter. Many electrical properties of networks of components (inductors, capacitors, resistors) may be expressed using S-parameter.S-parameter shown the level of feedback from the output of an amplifier to the input and therefore influences its stability.

The following is a representation of a signal wave in a two-port electrical-element.

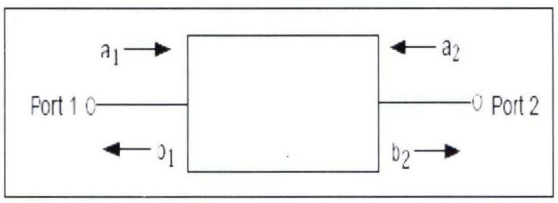

Fig.1 .Block diagram of S-parameter

Where

a_1 is the wave into port 1
b_1 is the wave out of port 1
a_2 is the wave into port 2
b_2 is the wave out of port 2

The S-parameters for this conventional element are defined in standard microwave textbooks as follows as:

$$b1 = S_{11}\, a_1 + S_{12}\, a_2$$
$$b2 = S_{21}\, a_1 + S_{22}\, a_2 \qquad (4)$$

The physical significance of the S-parameters is described as (5) – (8).Equation (5) is the reflection coefficient at port 1 when port 2 in terminated with matched load ($a_2 = 0$) while (6) is the reflection coefficient at port 2 when port 1 in terminated with a matched load ($a_1 = 0$).The attenuation of wave travelling from port 2 to port 1and from port 1 to port 2 is define in (7) and (8).

$$S_{11} = b_1/a_1 \text{ when } a_2 = 0 \qquad (5)$$

$$S_{22} = b_2/a_2 \text{ when } a_1 = 0 \qquad (6)$$

$$S_{12} = b_1 / a_2 \text{ when } a_1 = 0 \qquad (7)$$

$$S_{21} = b_2/a_1 \text{ when } a_2 = 0 \qquad (8)$$

S-parameters are defined with respect to reference impedance that is typically 50 ohms. For 50-ohm S-parameters with the 2-port element terminated with 50 ohms at each port, the S_{21} parameter represents the voltage gain of the element from port 1 to port 2.

Noise Figure is a measure of degradation of the signal-to-noise ratio (SNR), caused by components in a radio frequency (RF) signal chain. NR is defined as the ratio of signal to noise ratio at the output to that at the input.

For a 2-port circuit, the noise figure is the signal-to-noise ratio at the input, divided by the signal-to-noise ratio at the output. It has units of dB. The total noise is the transmitted input noise plus the noise contributed by the network. The transmitted input noise represents the portion of the incident thermal noise (kTB, where k=Boltzmann's constant, 1.380658 x 10^{-23} J/K, T=290 K, B=1 Hz) which passes through the system.

The noise factor of a system is defined as (9) where SNR_{in} and SNR_{out} are the input and output power signal-to-noise ratios, respectively.

$$F = \frac{\mathrm{SNR_{in}}}{\mathrm{SNR_{out}}} \tag{9}$$

The noise figure is defined as (10) where $\mathrm{SNR_{in,dB}}$ and $\mathrm{SNR_{out,dB}}$ are in decibels (dB). The noise figure is the noise factor, given in dB is expressed in (11).

$$NF = 10\log\left(\frac{\mathrm{SNR_{in}}}{\mathrm{SNR_{out}}}\right) = \mathrm{SNR_{in,dB}} - \mathrm{SNR_{out,dB}} \tag{10}$$

$$NF = 10\log(F) \tag{11}$$

If several devices are cascaded, the total noise factor can be found with Friis' Formula (12), where F_n is the noise factor for the n-th device and G_n is the power gain (linear, not in dB) of the n-th device.

$$F = F_1 + \frac{F_2 - 1}{G_1} + \frac{F_3 - 1}{G_1 G_2} + \frac{F_4 - 1}{G_1 G_2 G_3} + \cdots + \frac{F_n - 1}{G_1 G_2 G_3 \cdots G_{n-1}} \tag{12}$$

C. Circuit Description

The wideband LNA design objective is to choose the MOSFET parameters (i.e. size of Width and Length).The circuit is design for the wideband LNA with the ESD protection.

The general block diagram of a LNA is shown in Fig. 2, where two identical MOSFETs M_1 and M_2 form a cascode amplifier with a RC shunt-shunt feedback. In this work, the transistor M1 and M2 have the gate widths of 64μm and 52μm respectively. A flat S_{21} can be obtained above a wide bandwidth with low input/output of reflection coefficient by the proper adjusting of resistive component R_f and capacitive component C_f. Finally ,The value of R_c and C_f are 1.2kΩ and 1.1pF is selected.

For a better wideband matching, a source degeneration inductor of 0.2nH and a gate inductor of 2.7nH are also employed in the common source (CS) stage. A small inductor of 70pH is inserted between the CS and common-gate (CG) stages to further extend the bandwidth. To protect the gate oxide of during an ESD zap a large resistor of 5 k is used at the gate of CG. A capacitor of 1pF is added to provide an ac ground of the CG stage. To further the bandwidth and gain enhancement, the inductor of 9.3nH is used as inductive peaking. The transistors MB_1 and MB_2 are utilized as the output buffer to the 50 ohm measurement environment. [10]

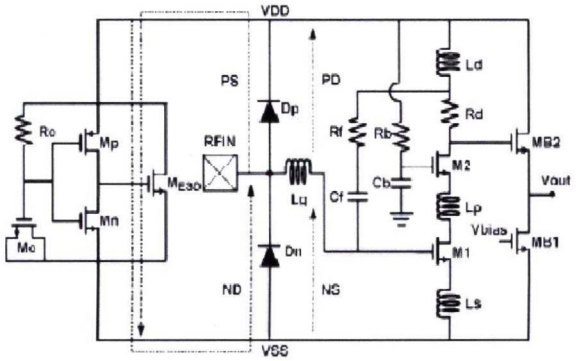

Fig.2 .Circuit topology for proposed ESD-Protected LNA

D. ESD Protection Circuit

The ESD protection blocks are also shown in Fig. 2, is build with a double-diode topology (D_p and D_n, together with the power clamp that designed by four transistors (M_n,M_p,M_c, and M_{ESD})and one resistor . The discharge paths for the four different ESD testing modes, i.e., positive (PD mode) and negative (ND mode) to V_{DD}, and positive (PS mode) and negative (NS mode) to V_{ss} are also indicated in the figure. In the PD and NS modes, the discharge current only flows through the diode, where as the discharge paths include both the diode and clamp in the PS and ND modes.

Double diodes at the input side of LNA are the important part for the ESD discharge paths and critical for the input matching network. To have sufficient ESD performance and almost no effect on the input matching network at the desired frequency band the two ESD diodes are optimize together with the power clamp. A large ratio of width and length (W=0.8 μm and L=30 μm) is proposed in this design to maximize the overall perimeter. With this structure, the ESD parasitic capacitance primarily exists in the bottom area and the current flows mainly through the edges of the diodes. The diode are also designed to utilize the maximum allowed contact and via density to reduce series resistance.

In addition, the MOS capacitor M_c and P-type poly resistor result in a RC time delay is to ensure M_{ESD} functions are correctly during an ESD event. M_{ESD} is designed by a multi-finger topology with a total gate width up to ~2000 μm to sustain a high ESD current level. This large size of M_{ESD} with a low on-resistance also allows the power clamp to consume less voltage budget under a certain current level, and thus relaxes the ESD diode design and requirement. [10]

III. RESULTS AND DISCUSSION

To validate the wideband CMOS LNA design concept, a 2.6-6.6 GHz LNA ESD-protected was implemented in a 0.18 µm RF CMOS technology. A complete graph of the $S_{11}$and S_{21} was illustrated in Fig. 3 and Fig.4.The graph of NF and P_{1dB} as shown in Fig.5 and Fig.6.The LNA was designed for a target that within the 3 dB bandwidth, the input return loss is greater than 13.0 dB, the peak power gain can achieve 13.8 dB, and the noise figure is in a range of 4.0 dB.

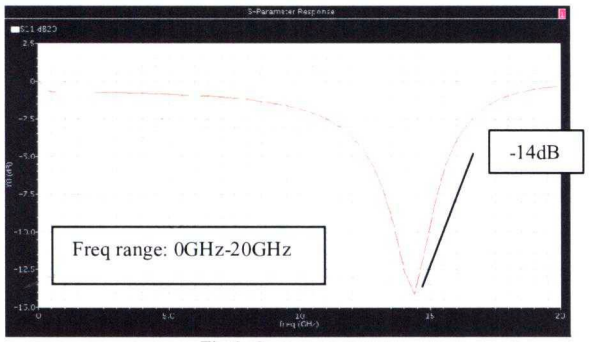

Fig.3. S_{11} parameter

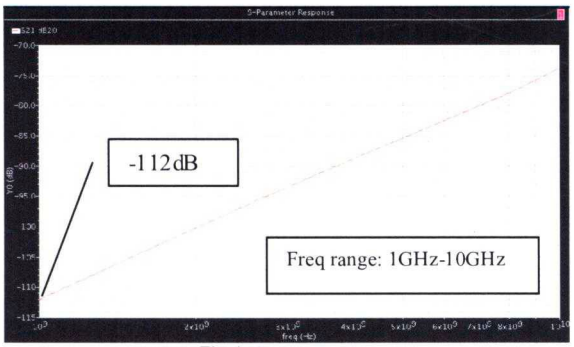

Fig.4. S_{21} parameter

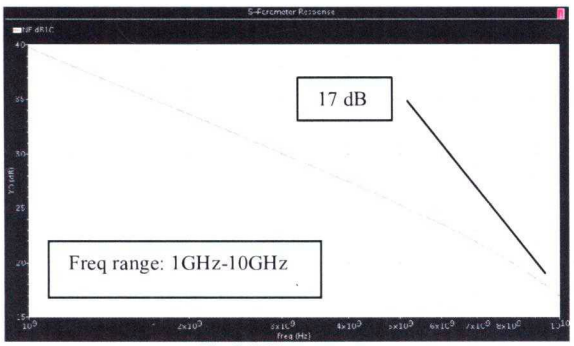

Fig.5. NF parameter

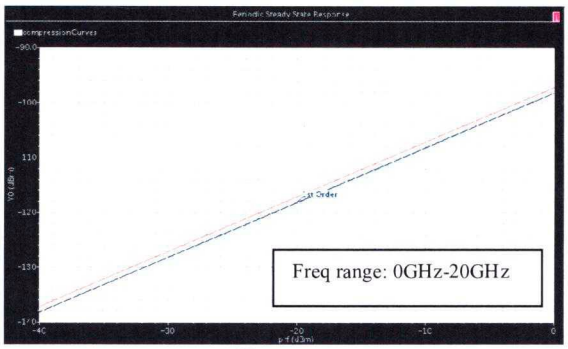

Fig.6. P_{1dB} parameter

The circuits is biased under a 1.2 V supply with an associated drain current of 5.7mA. With some modification on the core circuit of LNA, the impact of ESD block has been successfully minimized. Table I compares the published RF wideband LNAs with the considerations of ESD protection.

After done with the simulation, the results that obtain are almost achieving the requirement. The proposed LNA with HBM ESD need to achieve the requirement as within the 3 dB bandwidth from 2.6 GHz to 6.6 GHz, and the input reflection coefficient, S_{11} is below -13.0dB.Refered to the result, only the value for NF and S_{21} is slightly difference. Other parameters, such as S11 meet the requirement.

The CMOS technology and the software that use as an EDA tool will give a small impact to the value of the result that obtain. A long as the resulted value of the parameter is in the range of expected, the design can be proceed. The lab testing can be doing to confirm that the simulation result is achieving the requirement. This paper only proposed the simulation result.

Table 1
Performance Comparison of RF Wideband ESD-Protected LNA with Prior Art

Ref	Tech.(nm)	BW (GHz)	NF (dB)	S_{21} (dB)	S_{11} (dB)
This work	180 CMOS	2.6 – 6.6	17	-112	<-13
[1]	90 CMOS	0.1 - 8	3.4	16.0	<-10
[2]	90 CMOS	0.75 - 10	7.5	13.0	<-10
[9]	130 CMOS	3 - 5	3.6	25.8	-11
[3]	180 CMOS	0.5 - 3	3.8	16.0	<-10

IV. OPTIMIZATION S-PARAMETER

S-parameters are describing the electrical behaviors of linear electrical networks when undergoing various steady state stimulate by electrical signals. The parameters are useful for electrical and electronics engineering, and also communication systems design. Although it applicable at any frequency, S-parameters are mostly used for networks operating at radio frequency (RF) and microwave frequencies where signal power and energy considerations are more easily quantified than currents and voltages. S-parameters change with the measurement frequency so this must be included for any S-parameter measurements stated, in addition to the characteristic impedance or system impedance.

S_{11} and S_{21} is an important step in LNA circuit design. Through the process of EDA tools can be used iteratively to stimulate and refined the design. These tools combine accurate models with performance-optimization and yield-analysis capabilities. Optimizing the values of shunt and series, R and L is an iterative process with two goals:

a) The transformed load reflection terminates on the right gain at each frequency, and
b) The susceptance component decreases with frequency and the reactance component increases with frequency

First of all, a value for R_f need to be selected. If we start with the LNA design, R_f will be realized by an inductor Ls. Modified RF input circuit of mixer with source degeneration added for improving the linearity. Note in the LNA design these resistances are realized as loss-less inductors Ls. The inductive source degeneration proves good results when input impedance matching is considered. It provides creating a resistive part in addition to the reactive part seen at the gate of the input n-MOS transistor. Increasing the value of Ls helps to increase the resistive part of impedance, however, when small signal analysis is considered, it is obvious that increasing the source degeneration inductance results in lower gain. [11]

To optimize the S-parameter, some modifications in the circuit need to do. With some research, found that to vary the value of S_{21}, the resistive component R_f need to be adjusted. The proper adjusted for value of degeneration inductor, Ls the value of S_{11} will be effected. In this paper, the theory of S-parameter is applied. For noise figure NF, it will degrade if S-parameter improves their trade-off. So, as the S-parameter is changing, the values of NF are also affected.

The results of this optimization are shown in Table 2 and Table 3. Table 2 is the result of adjustable R_f and Table 2 for the adjustable of L_s.

Table2
Result of adjustable R_f

R_f (Ω)	S_{11}(dB)	S_{21}(dB)
0.2k	- 5.40	-112
4.4k	-4.40	-112
10.4k	-1.85	-112
50.4k	-0.46	-112

Table3
Result of adjustable L_s

L_s (H)	S_{11}(dB)	S_{21}(dB)
2.2n	-14	-87
6.6n	-14	-87
14.6n	-14	-101
24.6n	-14	-89

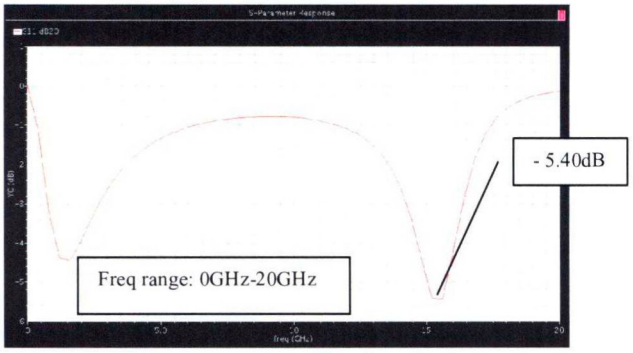

Fig.7. S_{11} parameter for $R_f = 0.2\ k\Omega$

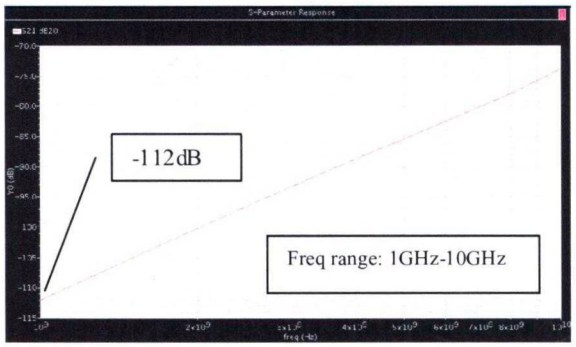

Fig.8. S_{21} parameter for $R_f = 0.2k\Omega$

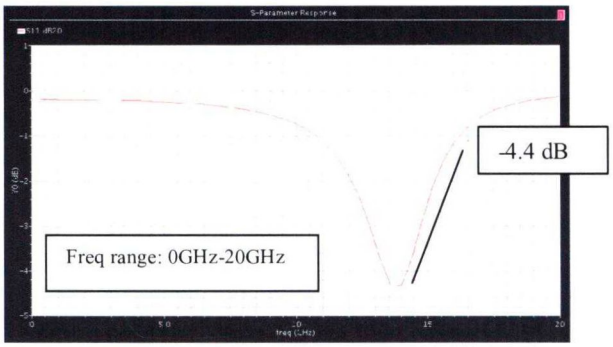

Fig.9. S_{11} parameter for $R_f = 4.4k\Omega$

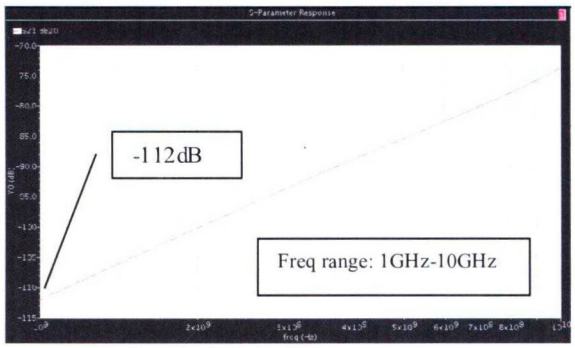

Fig.10. S_{21} parameter for $Rf = 4.4k\Omega$

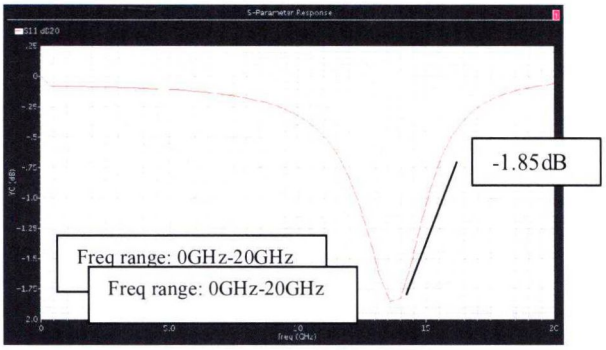

Fig.11. S_{11} parameter for $R_f = 10.4k\Omega$

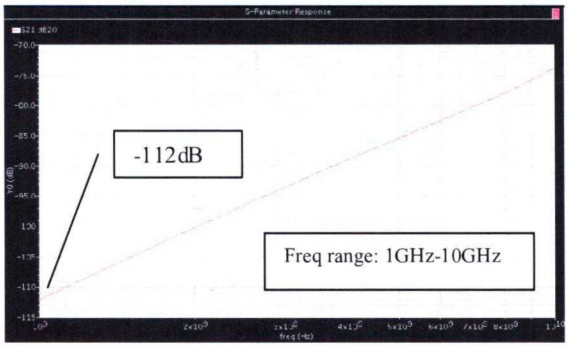

Fig.12. S_{21} parameter for $R_f = 10.4k\Omega$

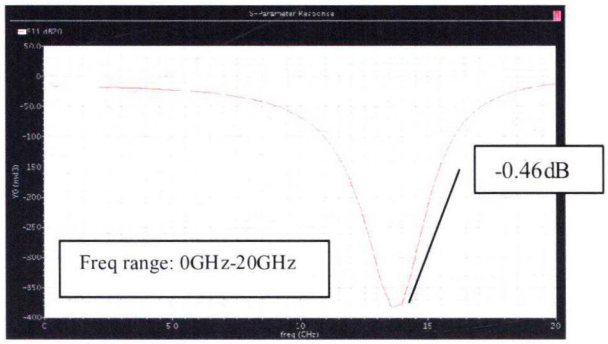

Fig.13. S_{11} parameter for $R_f = 50.4k\Omega$

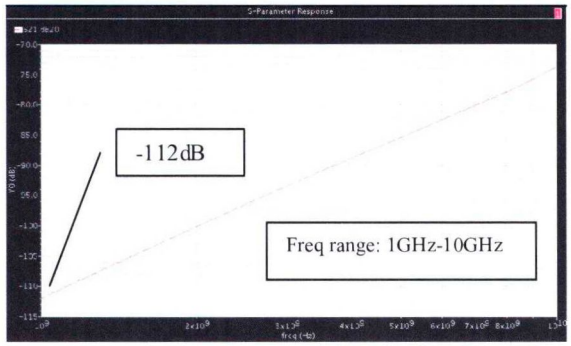

Fig.14. S_{21} parameter for $R_f = 50.4k\Omega$

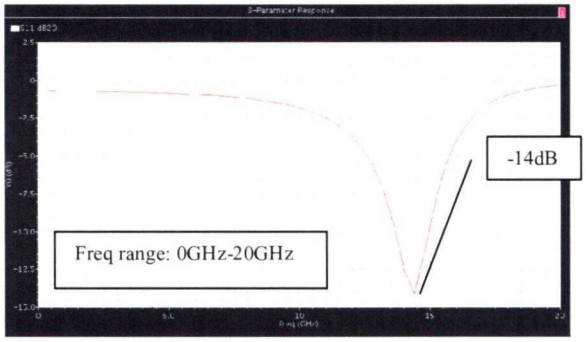

Fig.15. S_{11} parameter for Ls = 2.2nF

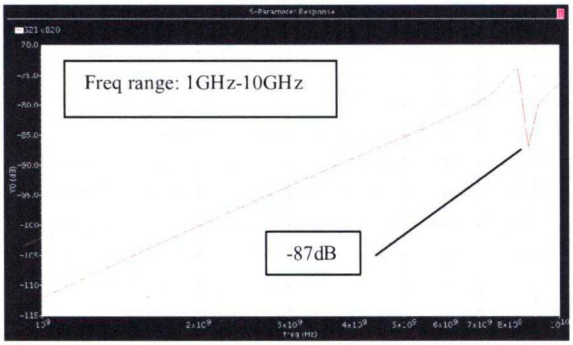

Fig.16. S_{21} parameter for Ls = 2.2nF

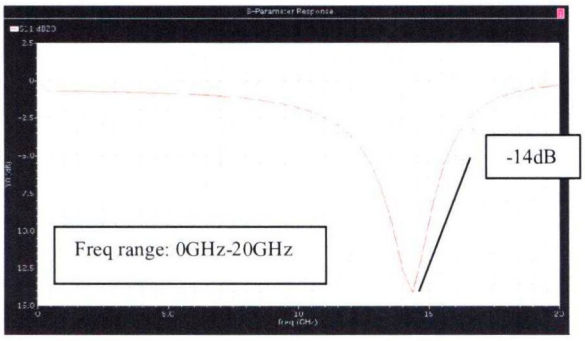

Fig.17. S_{11} parameter for Ls = 6.6nF

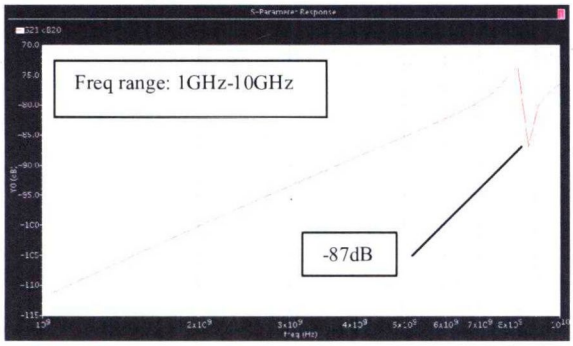

Fig.18. S_{21} parameter for Ls = 6.6nF

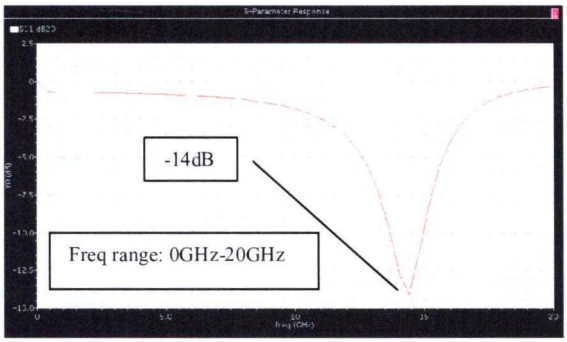

Fig.19. S_{11} parameter for Ls = 14.4nF

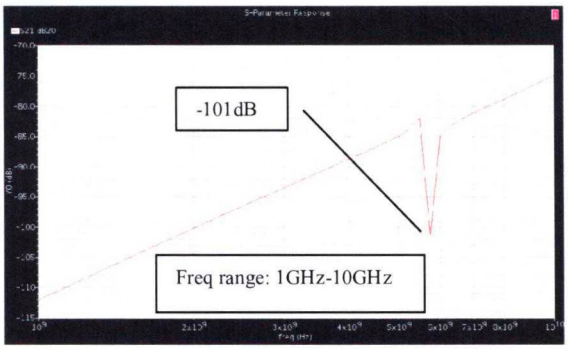

Fig.20. S_{21} parameter for Ls = 14.4nF

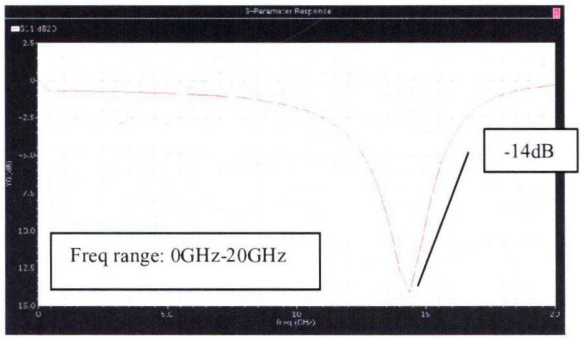

Fig.21. S_{11} parameter for Ls = 24.4nF

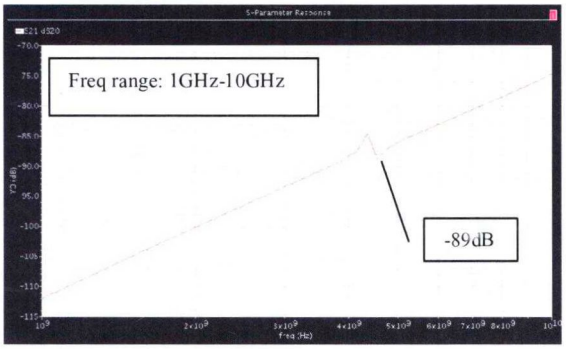

Fig.22. S_{21} parameter for Ls = 24.4nF

Fig.7 until fig.14 showed the graphs that obtain by simulation with the various values of R_f. On the other hand, Fig 15 until fig 22, showed the graphs that obtain by simulation with the various values of L_s. This value was chosen to know the effect of both components to the S-parameter. The range value for of R_f are from 0.2kΩ until 50.4kΩ while for L_s are from 2.2nF until 24.6nF.

To perform the analysis of this circuit, the range of frequencies need to be set. In order to perform better simulation, the range for S_{11} was chosen from 0GHz until 20GH while for S_{21} are from 1GHz until 10GHz.After this frequencies done to be set up, the simulation was proceed and the result are shown in Fig.7 until fig 22.

Refer to the Fig.7 until fig.14, for S_{11} there shown increasing in value as the value of R_f is increasing while for S_{21} the value are remain unchanged. For various values for L_s as shown in Fig 15 until fig 22, the value of S_{21} is changing while the value of S_{11} are remain unchanged.

Based on the graph and table for the adjustable value for both R_f and L_s, found that both of this value will effected the S-parameter value, S_{11} and S_{21}. It proves that as resistive component R_f adjusted, S11 will effected while degeneration inductor, Ls is adjusted the value of S_{21} will be effected.

As the value of R_f is increasing, the value of S_{11} will increase, so to get the better S_{11} the value of R_f need to be small. For S_{21} it will be decreasing, as the value of L_s is increasing. So, the value of L_s and R_f need to manipulate to get the requirement for S-parameter. This concept can be used to get the initial value for both components and optimize that value until get the suitable value.

The proper value need to be choosing to get the suitable specification. A flat S_{21}can be archive over a wideband bandwidth with low input and output of reflected coefficient .Moreover, a better value for S11 can be gain by verifying the value of resistive component, R_f.

V. CONCLUSION

In this paper, with the proposed analysis of the design of a wideband LNA with range of 2.6-6.6GHz LNA with HBM ESD Protection is demonstrated in 0.18μm RF CMOS Technology. Cadence Virtuoso is used as EDA tools to stimulate and refined the design. The analysis that performed in simulation was a successful analysis. The value of S_{21} is effected by adjusted the value of resistive component R_f while the S_{11} can be vary by adjusting the value of degeneration inductor, Ls.As the S-parameter is changing, the value of NF is also affected.

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