Implementation of Memristor using 0.13µm Technology in NAND and NOR for Hybrid CMOS Integrated Circuit

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***Abstract*— This project presents the use of nanoelectronic device known as memristor as an alternative device structure to CMOS in forming digital logic gates. The purpose of this research project is to develop a new model parameter based on actual measured data which all the parameter was described from the fabrication data. The I-V characteristic of the fabricated memristor is studied to form a Spice Macro model to represent the memristor and implemented into NAND and NOR gate. The NAND and NOR logical circuit will be designed and it will be simulated using LTspice software and producing designated layout using 0.13µm of Silterra technology in Mentor Graphic software and it will be compared with an existing spice model. The Hybrid CMOS NAND circuit designed, in comparison to conventional CMOS NAND using the Spice Macro model, is 68.90% times smaller and 47.90% times lower power consumption while the Hybrid CMOS NOR is 71.82% times smaller and 82.13% times lower power consumption than conventional CMOS NOR. This device will be beneficial to the technology as it is smaller with a high density and faster with low power consumption compared with the CMOS NAND and NOR.**

***Keywords*— Hybrid CMOS, Nanoelectronic Device, Memristor, Spice Macro Model**

I. INTRODUCTION

Moore's Law has stated that the size of transistor will be shrinking and the chip will be doubling every two years. However, the Moore's Law has it limit, due to the transistor that would eventually reach the limits of miniaturization at atomic levels. Therefore, the electronic designs need to shift to another alternative device that is not just smaller in size but increasingly capable [1]. Thus, a new nanoelectronic device being proposes by the name of memristor. The performance of digital circuits can be improved by combining transistor with memristor in a hybrid chip [1].

A memristor is the fourth basic two-terminal devices in the fundamental circuit elements which the other three are resistor, capacitor and inductor that usually known by people who have electronic background [2]. Figure 1 shows the relation of the four fundamental circuit variables, current, voltage, charge and flux would defined six elements which five have already defined as Resistor(dv=Rdi), Capacitor(dq=Cdv), Inductor(d ϕ =Ldi), q(t)= $\int$ i(T)dT, ϕ (t)= $\int$ v(T)dT and the 6th relation defines memristance as d ϕ =Mdq for memristor[2–5].

The memristor or known as "memory resistor" was first proposed by Leon Chua in 1971, where he predicted the existence of the 4th elements [1], [6]. From the 6th relation, the memristor has a memristance. Meaning that the memristor will retain its resistance level after the power is turned off or let it remember the last resistance it had before turned off[6]. For example, when the charge flows in one direction through a circuit, the resistance of the memristor increases and vice versa. When the applied voltage is turned off, charge flows will stops, thus the component will remember the last resistance it had. When the flow of charge regains, the resistance of the circuit will be the value when it was last active. Thus, making the memristor can be used as a non-volatile memory [1].

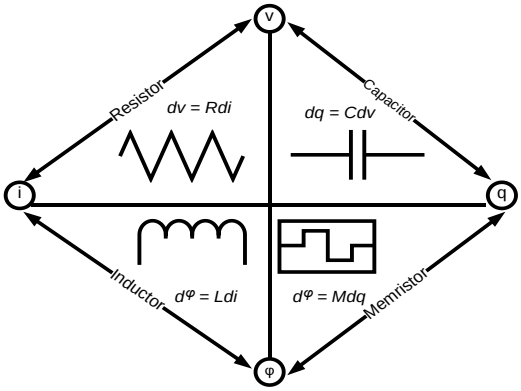


Figure 1. Four basic circuit elements and their relation (Adapted from[2]).

Based on Hewlett-Packard's (HP) of memristor, they managed to come out with a designed memristor based on titanium dioxide (TiO2) layer films [7]. It is a metal-insulator-metal structure which the two insulator layers, titanium dioxide (TiO2) are sandwiched by the two metal layers, platinum (Pt). The insulator layer can be represent by two type of resistance which is high resistance area and low resistance area. The high resistance area is slightly doped with oxygen vacancies become TiO2-x layer, other undoped region become TiO2 layer. The

oxygen vacancies are positively charged ion and make it conductive. Thus, the resistance width can be varied by the voltage [7]. The device established by HP is shown in Figure 2.

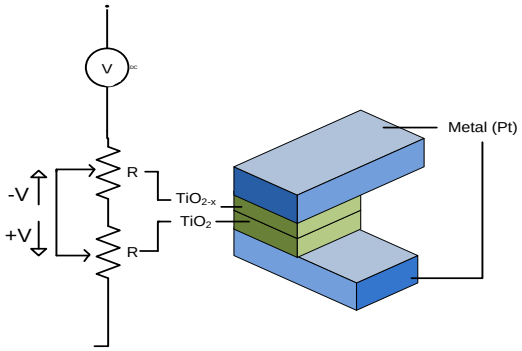


Figure 2. HP memristor model with a simplified equivalent circuit (Adapted from[8])

When a positive voltage is applied, the positively charged oxygen vacancies in the TiO_2-x layer are repelled, moving them towards the undoped TiO_2 layer. As a result, the boundary between the two materials moves, causing an increase in the percentage of the conducting TiO_2-x layer. This increases the conductivity of the whole device. When a negative voltage is applied, the positively charged oxygen vacancies are attracted, pulling them out of TiO_2 layer. This increases the amount of insulating TiO_2, thus increasing the resistivity of the whole device. When the voltage is turned off, the oxygen vacancies do not move. The boundary between the two titanium dioxide layers is frozen. This is the way memristor remembers the voltage last applied.

The switching behavior can be determined and demonstrated when there is interfacing between the Pt/TiO_2 and if there is a voltage applied through the terminal[9].

II. METHODOLOGY

A. Flow Chart

Figure 3 shows the flow chart of the project. First, the fabricated data were analyzed and existing Spice model from [10] were developed based on the mathematical function and Spice macromodel which then represented as subcircuit netlist. The existing Spice model parameters were also included in the netlist as an argument. For fabricated parameter, it is the same as existing Spice model which the parameter will become an argument in the subcircuit netlist. Therefore, the subcircuit can be used for both parameters either fabricated or existing Spice model by just replacing the parameter depends on the simulation wanted. The best fabricated data that has been chosen will be compared with the existing Spice data. Then, the Spice model and fabricated model were compared whether it meets the spec or not if yes, the project will proceed with designing the digital logic and layout. If not, the project will repeat the previous step. Lastly, the design is simulated and if it is success the project will come out with the good output where the spec and behavior is met.

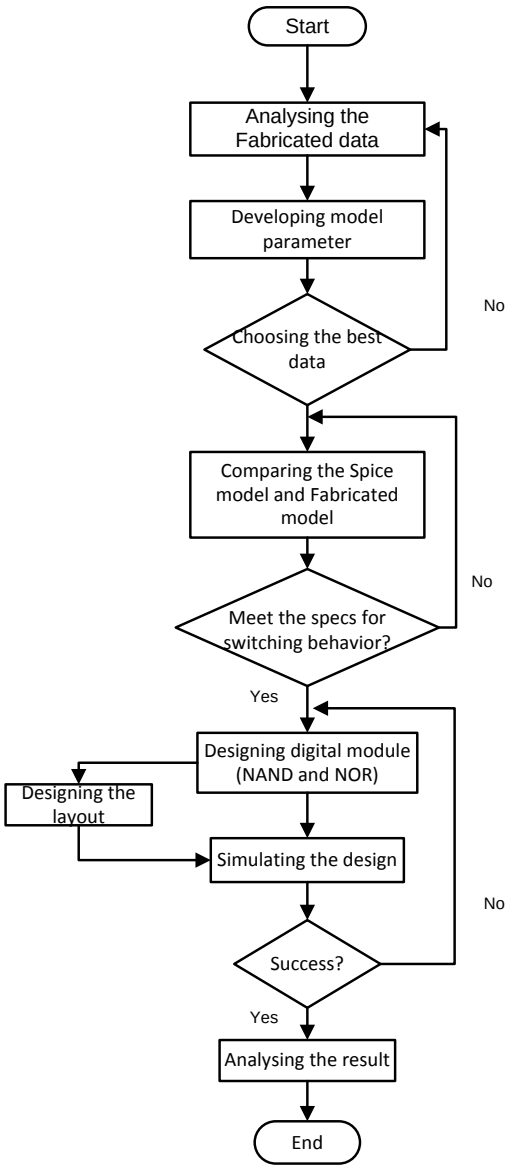


Figure 3. Flow Chart of the design

B. Model Mathematical Equations for linear model

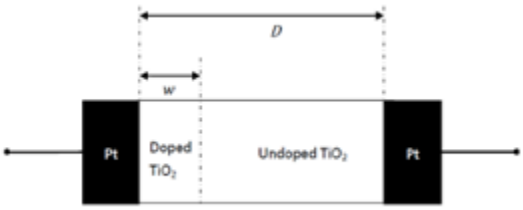


Figure 4. Memristor model (Adapted from[2])

Based on Figure 4, the width of doped region is labeled as w and the total length of the TiO_2 layer is labeled as D. The doped region behaves like low resistance which is denoted as R_{ON}. The undoped regions represent as high resistance which is denoted as R_{OFF}. The total resistance of the memristor, R_{MEM}, is actually a sum of the resistances of the doped and undoped layers. The high resistance R_{OFF} is much bigger than the low resistance R_{ON} which is usually with a ratio of 100 – 1000.

$$R_{MEM}(x) = R_{ON}x + R_{OFF}(1-x) \quad (1)$$

$$where \quad x = \frac{w}{D} \in (0,1) \quad (2)$$

x is defined as normalized state variable, the boundary is between zero and unity. The ON state and OFF state defines as unity and zero respectively.

From the ohm's law relation between the memristor voltages and current

$$v(t) = R_{MEM}(x)i(t) \quad (3)$$

Then, by insert equation (1) into (3). The voltage v(t) across the device will move the boundary between the two regions causing the charged dopants to drift. So, there is a drift ion mobility μv in the device. The change of the boundary is denoted as in (5).

$$v(t) = \left[R_{ON}x(t) + R_{OFF}(1-x(t))\right]i(t) \quad (4)$$

$$\frac{dx(t)}{dt} = \mu_V \frac{R_{ON}}{D^2} i(t) = ki(t) \quad (5)$$

To get x(t), then integrates the right side of equation (5) which then yields the following formula

$$x(t) = \mu_V \frac{R_{ON}}{D^2} q(t) \quad (6)$$

The equation (6) was inserted into equation (4) since usually R_{ON}<<R_{OFF} in order to obtain the Memristance, M(q).

The memristive system is depends on the charge passing through the device, the drift velocity, resistance of the device and the thickness of TiO_2.

$$M(q) = R_{OFF}\left(1 - \frac{\mu_V R_{ON}}{D^2} q(t)\right) \quad (7)$$

C. Windows Function for Nonlinear Model

The state equation (8), the passing current, and the resistance of doped area will affect the speed of the movement of the boundary between the doped and undoped regions [10].

$$\frac{dx}{dt} = ki(t)f(x), \qquad k = \frac{\mu_v R_{ON}}{D^2} \quad (8)$$

In order to analyze the behavior of memristor, window fuction is one of the important factors. By adding nonlinear window function known as f(x) can limit the boundary of state variable x within zero to one [11]. Nonliner dopant drift can be taken into consideration by introducing an appropriate window function f(x) into equation (4)[12].

In this paper, the window function that was choosen is Prodromakis. The function equation is as below:

$$f(x) = 1 - \left[(x-0.5)^2 + 0.75\right]^p \quad (9)$$

Control parameter of Prodomakis[10] window function can take any positive real numbers which allow a greater extent of flexibility of the window function.

D. Memristor SPICE Model

Simulation of model is defined by Macromodels which also can simplified the simulation elements and mathematical functions [10].

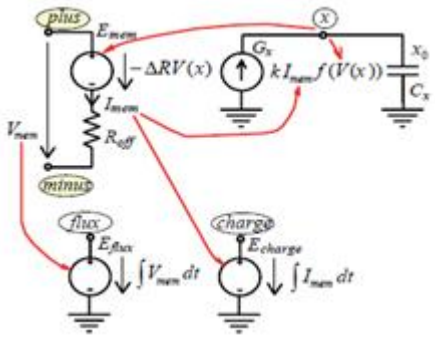


Figure 5. Structure of Spice Model from[10]

Figure 5 show the structure of the memristor model. The flux is calculated by integrating the voltage V_{MEM} and the charge is calculated by integrating the current I_{MEM} where V_{MEM} is the input voltage and I_{MEM} is the current through the memristor.

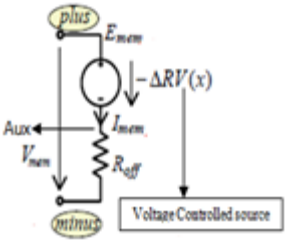


Figure 6. Resistive Part of Memristor

The circuit in Figure 6 is actually referred to total resistor R_{MEM}. From the equation $R_{MEM}(x)=R_{OFF}-x\Delta R$ where $\Delta R= R_{OFF}-R_{ON}$. R_{OFF} is placed in series with voltage source whose terminal voltage is controlled by the formula -xΔR. Resistive port is described by Ohm's Law, where $V_{MEM} =R*I_{MEM}=(R_{OFF}*I_{MEM})-(\Delta R*x*I_{MEM})$. Then, $R_{MEM}=R_{ON}*x + R_{OFF}(1-x)$. Term $R_{OFF}*I_{MEM}$ is the voltage drop at R_{OFF} due to memristor current and V(x)is the voltage of controlled source that depends on x (relative width of doped area)

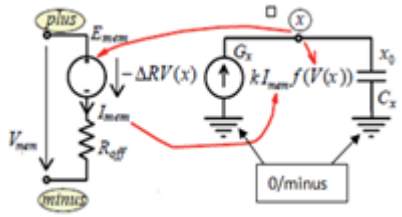


Figure 7. Differential Equation Part of Memristor

Figure 7 shows the differential equation modeling of the memrsitor. It consist a part of the voltage controlled source xΔR and the differential equation from equation (6) which serves as an integrator of the right side of the state equation (6) which is to get the value of normalize x.

G_X is a current source whose current is controlled according to the equation $I_{MEM}f(V(x))$ where V(x) is the voltage across the capacitor C_x and it models the normalized width x of the state variable between the doped and undoped layer. F(V(x)) is the window function, k is $\mu v R_{ON}/D^2$ and x_0 is the initial voltage of the capacitor [6].

From the mathematical equation and macromodel structure, the model can be implemented as a SPICE subcircuit[10]. The parameter in Table I will be pass into the subcircuit as arguments.

TABLE I. LIST OF PARAMETERS

Name	Parameter	Units
R_{ON}	Resistance of memristor for conducting state	Ω
R_{OFF}	Resistance of memristor for non-conducting state	Ω
R_{INIT}	Initial resistance of memristance	Ω
D	Thickness of memristor film	m
wf	The type of window function	-

E. Hybrid NAND and Hybrid NOR Gate

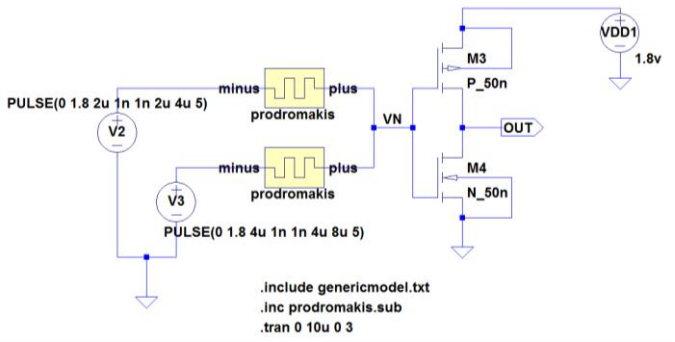


Figure 8. Schematic of Hybrid NAND

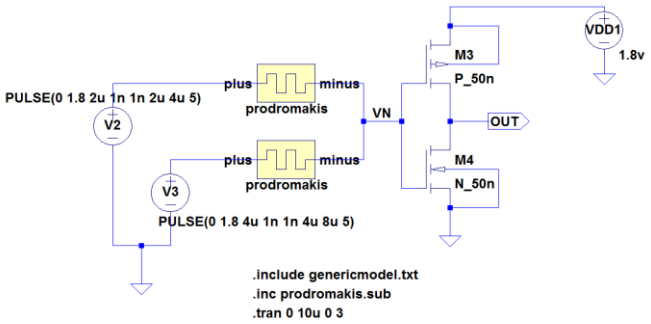


Figure 9. Schematic of Hybrid NOR

The combination of memristor with the transistor is called hybrid. Based on Figure 8 and Figure 9, the hybrid concept was applied on the NAND Gate and NOR Gate. In this project, the memristor type that has been chosen is the Prodromakis memristor, as it has the lowest power among the rest. The sizing of the transistors and the polarity of the memristor will the output of the hybrid to become a NAND Gate or a NOR Gate. A series of test is done to ensure that both NAND Gate and NOR Gate function well and behave accordingly to their specific behavior.

III. RESULT AND DISCUSSION

From memristor characterization process that have been done, the value of R_{ON} and R_{OFF} are taken from the I-V characteristic graph, while the sizing parameters are measured on the fabricated memristor to produce the table as seen in TABLE II and the data is used in Spice Model Parameter Simulation.

TABLE II. SPICE MODEL PARAMETER

	R_{ON} (Ω)	R_{OFF} (Ω)	R_{INIT} (Ω)	d (nm)	mu (f)	p
Fabricated model	1.55M	1.58M	1.55M	35	10	10
Existing Spice Model	100	16k	11k	10	10	10

From the data in the Table II, the simulation was run using LTSpice tools to check the I-V characteristic using SPICE model and also to check whether the hybrid configuration can be simulated on the NAND and NOR Gate. The simulation that was performed on these devices is on the power consumption and delay.

A. Memristor Structure based on Spice Model

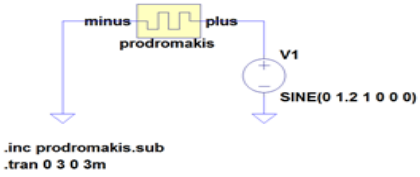


Figure 10. Schematic of Testing Memristor

The Spice model of the memristor was simulated as in Figure 10. The biased voltage is to show its hysteresis behavior.

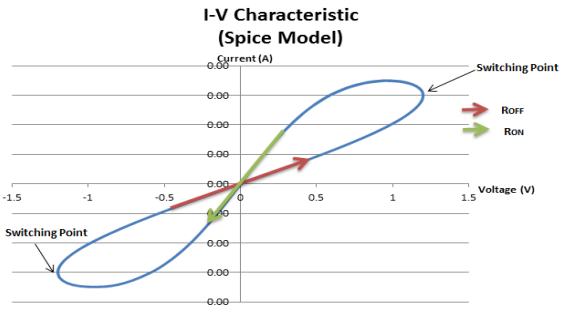


Figure 11. I-V Characteristic of Spice Model Memristor

The I-V characteristics curves are very important as they containing a lot of information regarding to the switching behavior of the memristor whether the devices is in ON or OFF states. Besides, the loops also representing and map the switching behavior of the device[13]. Figure 11 shows the simulation result of Spice Model memristor for Prodromakis window function [10]. The switching point from Ron to Roff happened at 1.2V while switching point from Roff to Ron happened at -1.2V.

B. *Memristor Structure based on Fabricated Model*

Same as the Spice model, the fabricated model also been simulated as in Figure 10. The different is the value of parameter in the subcircuit is referring the data that has been measured from the fabricated memristor.

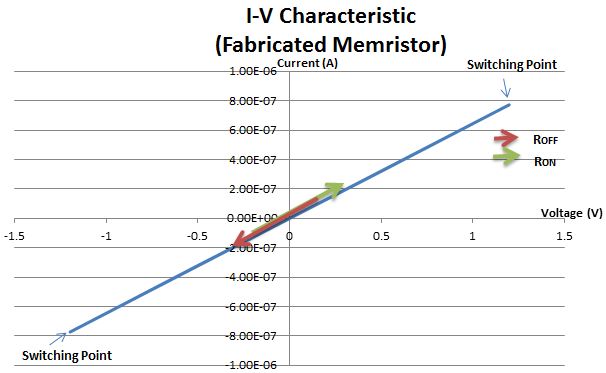


Figure 12. I-V Characteristic of Fabricated Model Memristor

Figure 12 shows the I-V characteristic curve for fabricated memristor. The operation of fabricated memristor is totally different from part A. Based on the actual measured data, the new spice model values are developed and give result as figure above. Based on the Table II, the R_{INIT} value is same as R_{ON} which means, the memristance is already in ON state. Thus, the direction of current flows in Figure 12 assumed different from Figure 11. The graph is look like a straight line because of the ratio of R_{ON} and R_{OFF} of the fabricated memristor is too small but is still have a small hysteresis loop and still function as memristor.

C. *Logic Gate Simulation*

a) *Spice Model Memristor*

Spice model memristor was obtained from the equation and macromodel circuit that has shown in the methodology which then was generated becomes subcircuit netlist. The parameter in the Table II for Spice model was adapted from [10].

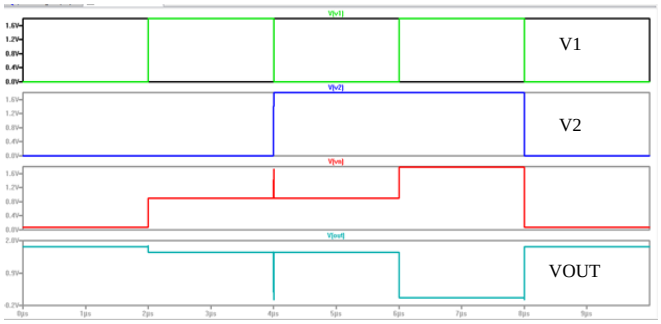


Figure 13. Simulation Waveform of Hybrid NAND gate for Spice Model memristor

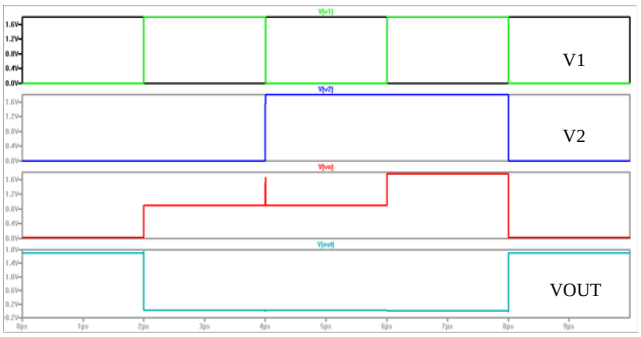


Figure 14. Simulation Waveform of Hybrid NOR gate for Spice Model memristor

Figure 14 and Figure 15 showing the simulation of waveform of Hybrid NAND and Hybrid NOR that run based on the Spice model.

b) *Fabricated Memristor*

The subcircuit for fabricated memristor is the same as Spice model memristor. The different is only the parameter that taken from the actual measured of fabricated memristor.

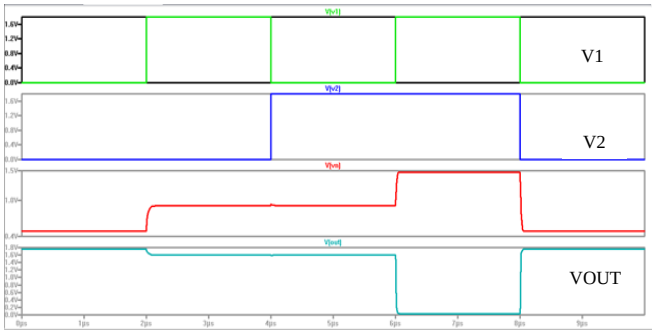


Figure 15. Simulation Waveform of Hybrid NAND gate for Fabricated memristor

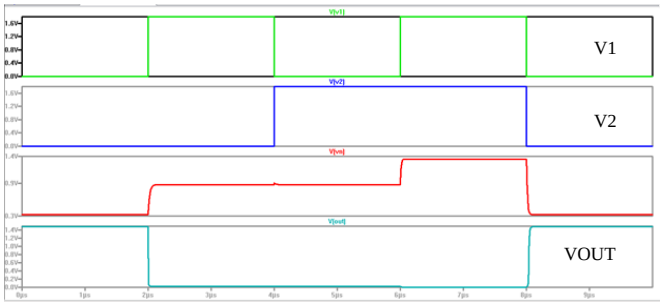


Figure 16. Simulation Waveform of Hybrid NOR gate for Fabricated memristor

Figure 16 and Figure 17 showing the simulations waveform of Hybrid NAND and Hybrid NOR that run based on the actual measured data of fabricated memristor.

Based on the both Spice model and Fabricated meristor simulation result, the output is produced as expected followed the truth table. Truth table for NAND and NOR logic gates was tabulate in Table III.

TABLE III. TRUTH TABLE

V1	V2	NAND	NOR
0	0	1	1
0	1	1	0
1	0	1	0
1	1	0	0

It is known that when the current flows into the logic gate through one of the inputs, the resistance of the memristive device will decrease to 'ON" state which known as low resistance. If both have identical inputs which is logic 1 or logic 0, the voltage drop between the inputs is zero. Thus, no current will flow through the circuit. So, output voltage is equal the input voltage. The increasing or decreasing resistance of memristor will change depends on the current that will flow from high voltage to the low voltage.

From Figure 14, Figure 15, Figure 16 and Figure 17, it could be seen from the output of the third graph is in the middle which not give a result either NAND nor NOR. This is because of delay time meaning that when V1='1' and V2='0' or vice versa the output waveform for these two conditions does not have enough time to change the resistance of memristive device to maximum or minimum resistance. Thus, the inverter is used in order to complete the logic family. This delay time actually happened for all configurations that have been tested. The desired result come out as expected followed the theory[14].

D. Delay Switching of Memristor

The switching process does not happen immediately after it reaches a threshold voltage. The memristor will take some time to switch from ON state to OFF state or vice versa due to the condition called delay switching. This is because the ion will take same time to reaches the boundaries of the device after the threshold voltage was reached. The delay time can be calculated using this equation:

$$T \approx \frac{D^2 Roff}{2\mu_v vRon} \tag{10}$$

Based on the equation (10) D is representing the width of the thin film, while μ_v is a migration coefficient and v is amplitude of the applied voltage. All of these values shown in Table II for existing spice model and fabricated model. By replacing these values into equation (10):

For Spice Model: $T \approx \frac{10n^2(16k)}{2(10f)(1.2)(100)} = 666.67ms$

For fabricated model: $T \approx \frac{35n^2(1.58Meg)}{2(10f)(1.8)(1.55Meg)} = 34.69ms$

From the calculation above, the time delay for fabricated model to turned from ON state to OFF state or vice versa approximately 34.69ms with sinusoidal input voltage amplitude ±1.8V. For Spice model, it takes for about 666.67ms to switch for sinusoidal input voltage with amplitude ±1.8V.

E. Comparison between CMOS Circuit and Hybrid Circuit of Spice Model and Hybrid Circuit of Fabricated Memristor.

TABLE IV. COMPARISON ON CMOS NAND CIRCUIT AND HYBRID NAND CIRCUIT

	CMOS Circuit	Hybrid Circuit (Spice Model)	Hybrid Circuit (Fabricated Model)	% Difference CMOS and Spice Model	% Difference CMOS and Fabricated Model
Area (μm^2)	60.96	18.96	18.96	-68.90	-68.90
Power (μW)	-97.26	-50.77	-50.86	-47.80	-47.90
Delay (ps)	133.05	141.87	7970	+6.22	+98.22

Based on the Table IV, it shows the % difference of CMOS NAND and Spice model and also % difference of CMOS NAND and fabricated model. The % difference in terms of area of layout and power consumption of Spice model and fabricated model, it is almost the same even though their parameter in the Table II are quite different. It can be seen that, the area of layout for both hybrid is reduced about 68.90% compared to the CMOS area of layout. Then, the power consumption of both hybrid is about 47% lesser than CMOS. Unfortunately, in terms of delay, both hybrid have a lot of difference. For hybrid Spice model, the delay is increasing about 6.22% compared to delay CMOS while the delay of hybrid fabricated model, the delay also increasing a lot which about 98.22% compared to the CMOS delay. Both

delays has slightly different maybe because of the parameter of R_{ON} and R_{OFF} of fabricated is bigger than Spice model.

TABLE V. COMPARISON ON CMOS NOR CIRCUIT AND HYBRID NOR CIRCUIT

	CMOS Circuit	Hybrid Circuit (Spice Model)	Hybrid Circuit (Fabricated Model)	% Difference CMOS and Spice Model	% Difference CMOS and Fabricated Model
Area (μm^2)	67.28	18.96	18.96	-71.82	-71.82
Power (μW)	-165.00	-22.04	-29.48	-86.64	-82.13
Delay (ps)	424.57	439.63	21990.00	+3.43	+98.00

Table IV shows the % difference of CMOS NOR and Spice model and also % difference of CMOS NOR and fabricated model. In this NOR configuration, the % difference in terms of area of layout and power consumption of Spice model and fabricated model same as NAND configuration which the area and power is reduced. As can be seen in the table, the area of layout for both hybrid is reduced about 71.82% compared to the CMOS area. Then, the power consumption of both hybrid is about 80% lesser than CMOS but in terms of delay for hybrid Spice model, the delay is increasing about 3.43% compared to delay CMOS. Same as NAND, the delay of hybrid fabricated model also increased about 98.00% compared to the CMOS delay.

F. Sizing

Based on the library Silterra 0.13µ Technology, the ratio of pmos and nmos has been calculated using ID equation where the current through both are considered same.

TABLE VI. SIZING OF CMOS TRANSISTOR

Ratio	VDD(V)	Power NAND (µW)	Power NOR (µW)
(2:1) x 4	1.2	23.85	1.89
	1.8	-6.16	-33.43
(2:1) x 10	1.2	23.37	1.10
	1.8	**-97.26**	**-165.00**

Table VI shows the sizing for CMOS transistor that was varied by different ratio and different VDD. The ratio pmos:nmos that has been calculated is 2:1. The original ratio then has been times in order to avoid DRC when designing the layout.

TABLE VII. SIZING OF MEMRISTOR

Ratio	VDD(V)	Power of Spice Hybrid NAND (µW)	Power of Fabricated Hybrid NAND (µW)	Power of Spice Hybrid NOR (µW)	Power of Fabricated Hybrid NOR (µW)
(2:1/2) x 10	1.2	-27.62	-28.15		
	1.8	-114.30	-144.81		
(2/2:1) x 10	1.2			-20.89	-21.53
	1.8			-90.44	-14.37
2.6:0.52	1.2	-11.03	-11.13		
	1.8	**-50.77**	**-50.68**		
0.52:2.6	1.2			-4.15	-4.29
	1.8			**-22.04**	**-29.48**

Table VII shows the sizing of the memristor which also was varied by different ratio and VDD. Memristor has unique way to sizing it due to hybrid architecture. When the memristor connected with the CMOS transistor, the behavior of the logic was determined by the transistor. For the NAND memristor, the pmos must be greater than nmos. Meanwhile, for the NOR memristor, the nmos must be greater than pmos. Besides that, the VDD also related in order to determine the behavior of memristor. The VDD must be more than 1.2v which is 1.8v if not, the memristor will not act as memristor. It can be conclude that, for sizing of memristor the smaller size the better output, but the ratio must be maintained and the sizing cannot be too small until memristor lose its behavior. Based on both Table VI and Table VII, the sizing was choosing by referring the best output of memristor.

G. Layout

Figure 17 is the proposed designated layout of the memristor. All the measurement that was designed on the figure was referring illustration in [1].

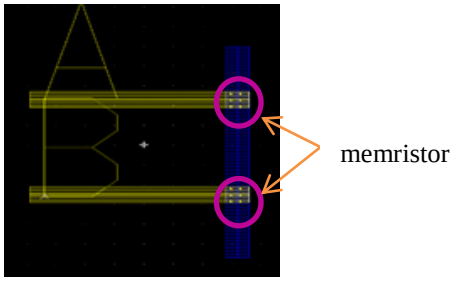
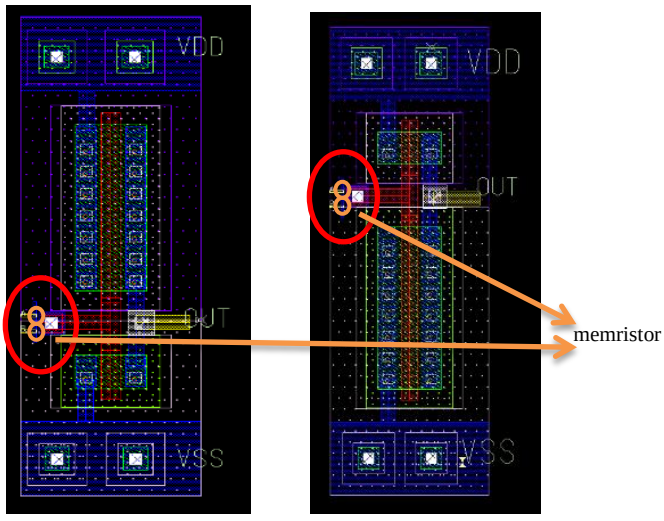


Figure 17. Layout of the memristor

As stated in the introduction and methodology, the memristor will be combined with CMOS transistor to performed a NAND and NOR gate. Therefore, this layout will be combined with transistor layout which will be done by using Mentor Garphic software.



(a) (b)

Figure 18. (a) Layout of the Hybrid NAND, (b) Layout of Hybrid NOR

Figure 18 (a) and (b) are the layout of Hybrid NAND and Hybrid NOR after combining the memristor layout with the transistor layout. As can be seen, the circle at the layout is the memristor which have a lot of decreasing of area of layout compared to the transistor.

IV. CONCLUSION

As a conclusion, a new spice model parameter value has been created based on the actual measured data and been compared with an existing spice model. The device behaviors are linked in between the fabrication and circuit performance. The fabricated Hybrid circuit has shown that it has a better performance in terms of power consumption and the size of the layout. Based on the result, the idea of using Hybrid circuit can be proposed as an alternative solution for conventional CMOS sizing limitation. This research can be a reference in producing nanoscale electronic device

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