# Investigation of Doping Techniques on the Silicon Based Capacitor

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***Abstract*- This technical paper investigates the effect of doping techniques, type of dopant species and plate size on the capacitance density of a silicon based capacitor. The substrate of the silicon wafers were highly doped using either solid source (SS) or spin-on dopant (SOD) method. Three different diffusion temperatures were used in this experiment which are 900°C, 1000°C and 1050°C. Results show that the diffusion by spin-on dopant gives a higher capacitance density compared to diffusion by solid source and larger plate size would contribute to a larger capacitance value. In addition, the experiment also shows that n-type wafer heavily doped with phosphorus exhibits a higher capacitance density.**

***Keywords*- *solid source, spin-on dopant, capacitance density, segregation, pile-up, heavily doped bulk substrate***

## 1. INTRODUCTION

In general, capacitors have a dielectric that is sandwiched between a pair of parallel electrodes, and function to store electricity. The characteristics of the capacitors largely vary depending on the kinds of dielectrics used. Capacitance has been found to be inversely proportional to the thickness of the dielectric material, thus thin film capacitors are generally seen as a preferable means to achieve high performance [1].

As the electronic circuits are being miniaturized to an increasing degree as a result of advances in the integrated circuit technologies, the miniaturization of capacitors that are indispensable in the integrated circuits as circuit elements is also becoming especially significant [2]. To achieve large-capacity capacitors, the thickness of an insulating layer interposed between the capacitor electrodes should be reduced. The silicon based capacitor in this experiment resembles the concept of a parallel plate capacitor using silicon dioxide as the dielectric layer [3].

The main objective in this paper is to study the effect of different doping methods such as solid source (SS) and spin-on dopant (SOD), type of dopant species used and the capacitor plate size in relation to the capacitance density. These parameters were of interest because of the effect on the capacitance density can be seen and investigated when the values are varied. From previous studies, it was known that different doping concentration and impurity types introduced into the silicon can affect the thickness of the oxide layer grown during the thermal oxidation process. To strengthen the reason for choosing the variables, the capacitance (1), and the capacitance density (3) equation of a parallel plate capacitor were referred. Parameters such as the separation distance between the plates,*d* is related to the oxide dielectric thickness and the plate area,A is related to the sizes of the capacitor . The diffusion temperatures used for the diffusion process of phosphorus and boron impurities in the silicon substrate were 900°C, 1000°C and 1050°C.

The silicon substrates were heavily doped with the same dopant type as the original wafer type to increase the majority carrier concentration in the substrate regardless of the doping method used. Hence, the contribution of the minority carriers in the substrate has a minimum effect on the capacitance density [4].

## 2. METHODOLOGY

The methods and processes conducted throughout the experiment are clearly stated in Fig. 1. Four inch silicon wafers with (100) orientation were used in the experiment. In order to observe the difference in characteristics of the p-type and n-type capacitors, the initial fabrication step was divided into these two groups. Throughout the fabrication, the samples undergo diffusion, oxidation and also metallization processes.

Firstly, the wafers had to be cleaned by using the wet cleaning procedure. This was done by first soaking the samples into a Buffered Oxide Etch (BOE) solution which is a mix of hydrogen fluoride (HF) and ammonium fluoride ($NH_4F$), then rinsing it through de-ionized water (DIW). Ionic contaminants in water can deposit on the wafer and cause device degradation. These steps were necessary in order to remove any dust or native oxide particles.

Regardless of the doping methods and dopant types used, a flow of $N_2$ gas of 10 standard liter per minute (slm) was introduced in the diffusion furnace in order to prevent impurities from depositing on the silicon wafer. Nitrogen gas carries unwanted impurities away from the furnace.

During the metallization process, a thin Aluminum layer was deposited on the grown oxide layer using evaporation in low pressure method. The equipment used was the Modu-Lab PVD.

To study the effect of different plate sizes on the capacitance value, three different sizes of capacitors were fabricated which had the values of P1= 1.9516cm$^2$, P2= 0.7903cm$^2$, P3= 0.4032cm$^2$. The mask used in this experiment was designed by using the TurboCAD Designer15 software.

Positive type photoresist was used in the experiment. The resist was deposited on the aluminum by using the Laurell Model WS-400E single wafer spin processor. The spin speed was set to 1500rpm for 30s. The samples were then placed on the hot plate for the softbake process at the temperature of 100°C for

5 minutes. After that, the sample was exposed to UV light for 50s. Next, the photoresist was developed by dipping the sample into the resist developer. The final lithography process is to hardbake the sample for 7 minutes at a temperature of 110°C.

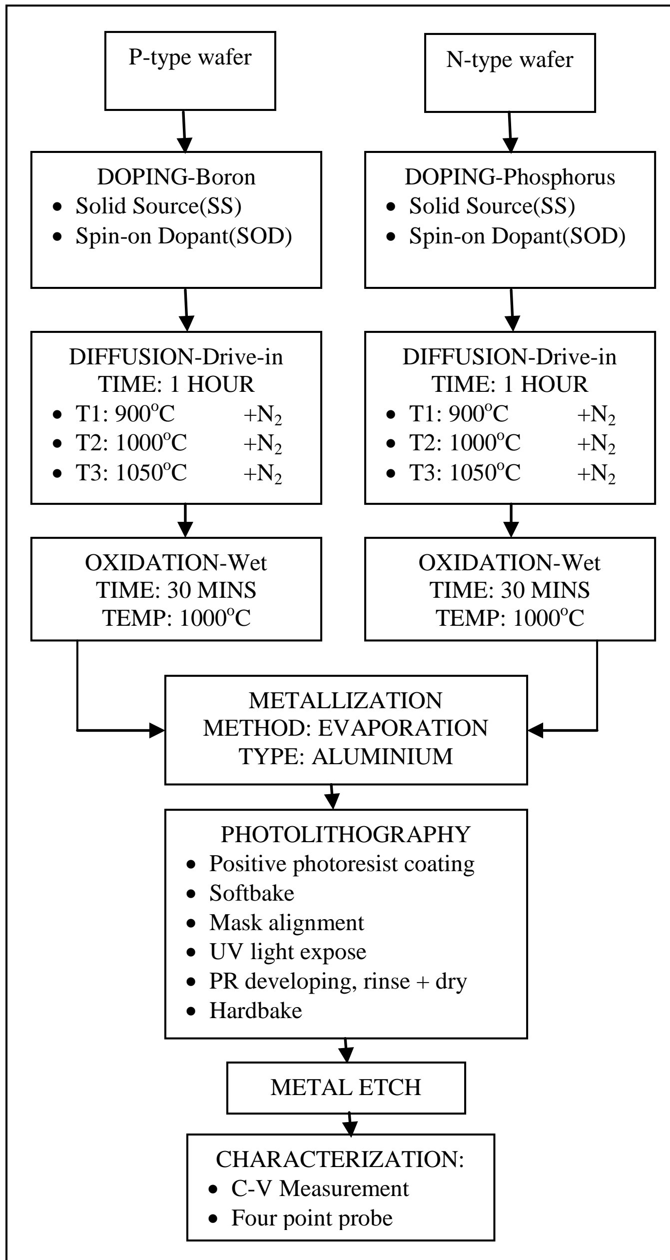



Fig. 1 Flowchart of the experimental procedure

To obtain the desired capacitor sizes, the aluminum layer were then etched by submerging the samples into the aluminum etch solution at 65°C for 90 minutes. It was necessary to move the samples up and down in the aluminum etch solution in order to obtain a more uniform etch of the aluminum layer.

Low frequency CV measurement was conducted on the samples to obtain the CV plot in order to study the electrical properties of the capacitor. This test was performed using the Keithley 595 Quasistatic CV meter and the Modu-Lab Benchtop CV software. Voltages between -3V to +3V were swept on the metal gate of the capacitors. The data of capacitance at certain voltages was then saved from the software and extracted into Microsoft Excel for analysis.

## 3. Results and Discussion

Throughout this experiment, it should be noted that all the values of capacitance density were taken when the voltage applied was +1V. Upon using MathCAD for simulating a MOS capacitor with similar characteristics of the fabricated capacitors, it has been found that the CV plot for all the samples shared a similar trait where all of the capacitors fabricated would operate in their accumulation phase at +1V.

### *3.1. Effects of Doping Techniques*

To investigate the effects of different doping techniques used to diffuse boron and phosphorus on the capacitance density, graph Fig. 2 (a) and (b) were plotted.

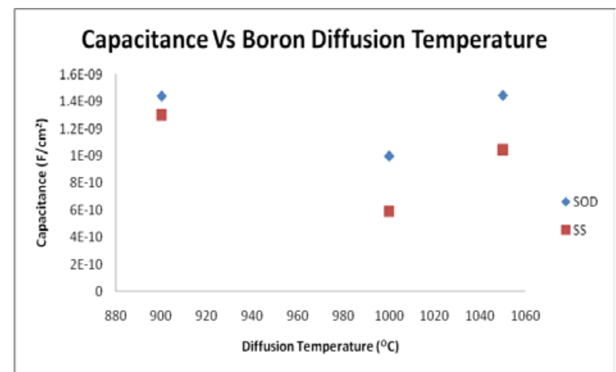
The capacitance equation, C of a parallel-plate capacitor:

$$C = \varepsilon_r \varepsilon_0 \frac{A}{d}, \qquad (1)$$

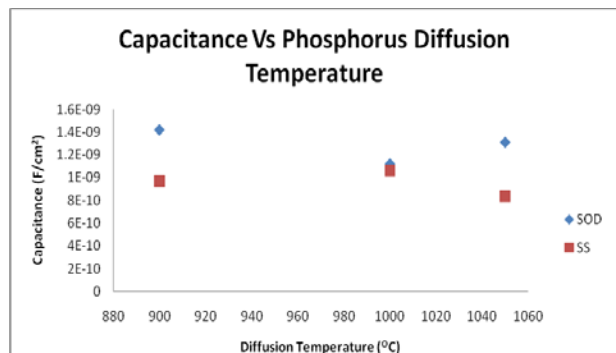
$$C = \frac{dq}{dv} \qquad (2)$$

and the capacitance density:

$$\frac{C}{A} = \frac{\varepsilon_r \varepsilon_0}{d} \qquad (3)$$




(a)




(b)

Fig. 2 Capacitance against diffusion temperature
(a) Si doped with boron (b) Si doped with phosphorus

From Fig. 2 (a) and (b), it can be seen that by using the SOD method, the capacitance density obtained would be higher compared to the capacitance density of the capacitors fabricated using the SS method.

This phenomenon can be explained by the fact that diffusion by SOD method would introduce a lower impurity concentration in the silicon substrate compared the higher impurity concentration introduced by using SS.

It was found that the oxidation rate increases with increasing dopant concentration [5]. This means during thermal oxidation, the oxide thickness over the heavily doped regions may be greater than over the lightly doped region. From the findings, it can be said that using the SOD method would give a smaller oxide thickness and in turn a larger capacitance density.

Based on (1) and (3), it can be deduced that any changes to the value of distance between the capacitor plate,*d* will in turn affect the capacitance ,C. The main focus upon discussing this factor is the difference in the oxide thickness grown during the wet oxidation process. Taking the oxide thickness as the separation distance between the plates, d it is shown that the value of capacitance is inversely proportional to *d*.

Reasons for the difference of impurity concentration introduced in the substrate between the two diffusion methods are explained in the next subsections.

*3.1.1 Spin-On Dopant (SOD)*

Silicate Spin-On Glass (SOG) may be doped with phosphorus or other dopants. A doped SOG is often called Spin-On Dopant (SOD) when it is used as a diffusion source. The viscosity of the silicate SOG solution is fairly low. As a result, the obtained layer by each spin is very thin. The planarity is generally poor and it normally requires multiple spins to achieve good planarity [6].

Furthermore, diffusion of SOG doped with boron or phosphorus could make the film hygroscopic and when react with water at room temperature, will lead to the formation of volatile compounds at the diffusion temperature. In the consideration of boron, this gives rise to variation in the amount of $B_2O_3$ reacted with silicon. Thus great care must be taken to keep the deposited wafer from coming in contact with moisture if reproducible diffusions are to be achieved [6].

In addition, one of the factors that control the deposition process is the diffusivity of the impurity atoms [7]. In terms of the diffusion rate, it is known that matters in gaseous form would diffuse much faster than matters in the form of liquids or solids. Therefore, this could also be related to the reason why the diffusion of impurity atoms into the substrate using the SOD method is slower.

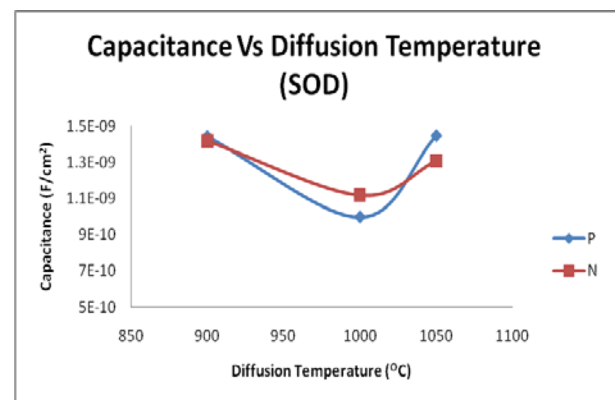
*3.1.2 Solid Source (SS)*

The SS doping method introduces a more purely doped impurity species in the semiconductor substrate. During the diffusion process, a small flow of $N_2$ was used to prevent backstreaming of airborne contaminants into the diffusion tube and due to this reason, the impurity concentration on the surface of the substrate will be higher because of the uninterrupted flow of impurities [7].

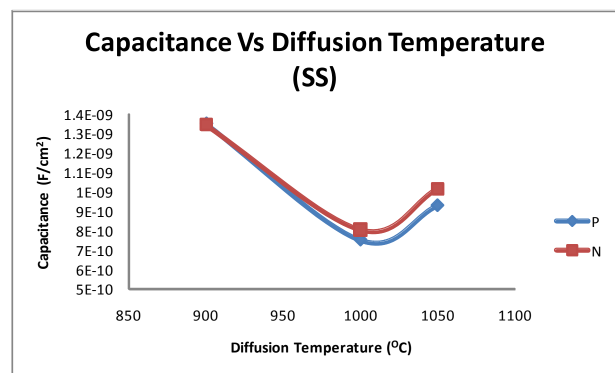
In terms of p-type doping, high concentration of boron can be transported from the BN disc using a process termed hydrogen injection. Hydrogen is streamed to the discs to form a $HBO_2$ vapor which has a high vapor pressure, therefore significant surface concentrations of boron on the Si can be achieved with this technique [7].

*3.2. Effects of Impurity Types*

The next factor that will be discussed is the effect of dopant species type used to dope the bulk substrate. It was mentioned in the procedure that the n-type wafer was heavily doped with phosphorus while the p-type wafer was heavily doped with boron.




(a)




(b)

Fig. 3 (a) Capacitance against SOD diffusion temperature for boron/phosphorus doped wafer
(b) Capacitance against SS diffusion temperature for boron/phosphorus doped wafer

As previously discussed, the thickness of the oxide layer grown is strongly linked with the impurity concentration in the silicon substrate. The overall opinion on the mechanism of the oxide growth is that it occurs at the interface of the $Si\text{-}SiO_2$ and that initially it is reaction rate limited by the interface, resulting in a linear growth relation. After oxide thickness progresses, the diffusion-limited process of the oxygen traversing through the oxide limits the growth rate and the reaction becomes inversely dependent on the oxide thickness. This results in a parabolic growth rate [8].

During the thermal oxidation process, dopants redistribute between the growing oxide and silicon as the Si-$SiO_2$ boundary moves into the silicon bulk and can cause considerable changes in the impurity in silicon near its surface [9].

The physical "tendency" of dopants to diffuse either in oxide or silicon is quantified by the segregation coefficient, m.

$$m = \frac{\text{Equilibrium concentration of impurity in Si}}{\text{Equilibrium concentration of impurity in SiO2}} \quad (4)$$

Fig. 3 (a) and (b) depicts the p-type substrate doped with boron exhibiting an overall lower capacitance density compared to the n-type substrate doped with phosphorus at higher diffusion temperature. This result will be discussed in terms of changes occurring on the thickness of the oxide dielectric layer. In turn, relating to variations on the distance between the capacitor plate,*d* in (1) and (3). Since the thermal oxidation process in this experiment was conducted at 1000°C with the presence of $H_2O$, it is known that the main mechanism for the oxide growth at this temperature is related to the parabolic growth rate [9]. In the discussions below, it is important to keep in mind that at higher diffusion temperature, the impurity concentration of boron or phosphorus at the Si-$SiO_2$ interface will also increase.

The results also shows a "V" shaped relation between each of the three points. This relation can best be explained by referring to the maximum solid solubility of the impurities that can be put into the wafer. From the graph of concentration against diffusion temperature for the solid solubility of impurities in silicon, it can be seen that the solubility of impurities including boron and phosphorus initially increases with temperature (900°C) and then begins to decrease (1020°C) as the crystal melting temperature is approached. This is known as retrograde solubility [7]. It was previously found that the melting temperature for silicon in the form of solid is approximately at 1414°C.

*3.2.1. Phosphorus Doped Silicon*

Since phosphorus has a high segregation coefficient of approximately ~10, it has the tendency to "pile-up" at the silicon surface during thermal oxidation, while their concentration in the oxide remains low [7]. Thus, making the oxide layer more difficult to move into the silicon substrate and limiting the growth of oxide dielectric layer.

At 1000°C, a high bulk concentration of phosphorus causes little change in oxidation rates which means higher capacitance density. This is consistent with the findings of Haas and Gray [8]. Due to the "pile-up" effect, the oxide produced will be essentially $SiO_2$ and subsequent oxygen diffusion through it will not be significantly affected.

In Fig. 3 (a), it can be seen that at the diffusion temperature of 1050°C, the capacitance density of the boron-doped silicon is higher compared to the phosphorus-doped silicon. This slight deviation might have been caused by the doping method used. The deposition of the boron spin-on dopant might have been poor and in turn leads to a lower impurity concentration in the substrate.

*3.2.2. Boron Doped Silicon*

The cause of oxidation rate dependence on boron is different from that of phosphorus. At the oxidation temperature of 1000°C, boron with the segregation coefficient of ~0.3, tends to segregate into and remains in the silicon dioxide during thermal oxidation. Hence, the bond structure of the silicon dioxide weakens as a result of the large boron concentration. This in turn, allows both $O_2$ and $H_2O$ to enter the silicon dioxide more easily and also to diffuse through it more rapidly, thereby leading to enhanced oxide growth [7] which in turn, obtaining a lower value of capacitance.

The decrease in capacitance value from the temperature of 900°C to 1000°C is shown in Fig. 3 (a) and (b). The main reason for the decrease in capacitance value is because the oxide thickness in both boron-doped and also phosphorus-doped silicon has increased. The result in Fig. 4 (b) agrees with the observation made by Deal and Sklar (1965) which shows that at the oxidation temperature of 1000°C, substrates highly doped with boron will obtain a higher oxidation rate compared with high boron-doped substrate [10]. This is because there will be more boron impurities available in the oxide layer due to the property of segregation. As explained before, the structure of the silicon dioxide will have more tendency to be weakened.

3.3. Effects of Plate Size

The final characteristic studied was the effect of the capacitor sizes on the capacitance. Three different sizes of capacitor were fabricated.

From Fig. 4, it can generally be interpreted that the largest capacitance density is given by the largest capacitor size, P1. Reason for this matter is best explained by the well-known equation for capacitance (1). Where, A is the area of the conducting plates between the dielectric and is directly proportional to the capacitance density.

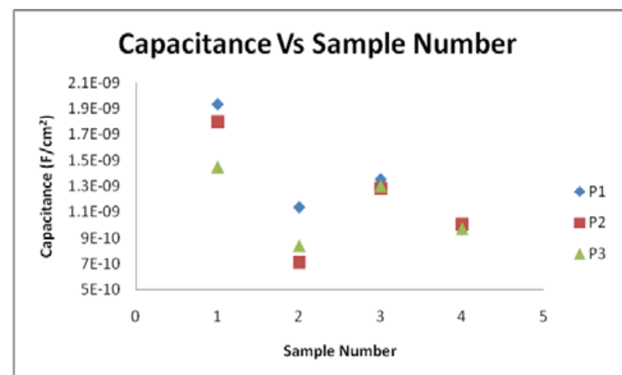



Fig. 4 Capacitance value against sample number
P1= 1.9516cm$^2$, P2= 0.7903cm$^2$, P3= 0.4032cm$^2$
S1= P-type SOD, S2= N-type SOD, S3 = P-type SS, S4= N-type SS

Analogous to the operation of a parallel plate capacitor, the charge passing through the top plate (metal), cannot pass through to the other plate (bulk substrate) because the presence of the silicon dioxide dielectric. Instead a charge of +q is stored on the top plate and this will cause a charge of –q to be formed at the bottom plate [11]. The gate charge form at the metal gate is equal and opposite to the bulk charge in the silicon substrate

[12]. Taking that P1 has the largest metal plate area, it relates to the highest value of capacitance because of its capability to store more charge on the plate. This will then be followed by an increase in the electric field and eventually the capacitance.

Experimental data also shows that the capacitance density obtained by the SOD doping method is more affected by the plate size because the differences in capacitance value is more obvious for P1, P2 and P3. Reason for this is because the contact between the oxide and aluminum metal is stronger due to the relatively high average roughness of the doped surface using SOD [13].

## 4. CONCLUSION

It is clear that various parameters such as doping methods, type of dopant species and plate sizes do affect the capacitance of a silicon based capacitor. It was shown that diffusion by SOD gives a higher capacitance density compared to diffusion by SS and that a larger plate size would contribute to a larger capacitance. The experiment also shows that n-type wafer heavily doped with phosphorus exhibits a higher capacitance density. Several properties that affect the thickness of the oxide layer grown such as the segregation and oxidation mechanism at specific temperatures will also affect the capacitance density. It can be concluded that the variations of the mentioned parameters, generally alters the variables in the equations for capacitance (1), (2) and (3).

For the future development of the silicon based capacitor, various considerations should be taken during the fabrication process. The characteristics of the silicon based capacitor could be improved by considering different "drive-in" and thermal oxidation duration. Since dry oxidation is known to give a better oxide quality, it could also be the chosen as the oxidation method in future. This is because the oxide dielectric plays a critical role in the characteristics of the silicon based capacitor. Furthermore, the type of oxide could also be varied to substitute the $SiO_2$ dielectric layer presently used. Hence, further study would also be needed to determine segregation properties of impurities in these dielectric types.

## ACKNOWLEDGEMENT

The author would like to express his deepest gratitude towards his supervisor Mr. Ahmad Sabirin Zoolfakar, co-supervisors Mr. Azlan Zakaria and Mrs. Maizatul Zolkapli for the guidance and technical support. The author would also like to thank all of the individuals who were involved directly and indirectly and making it possible for him to complete the experiment successfully.

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