Investigation of Electrical Characteristics of Fully-Depleted SOI Device

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***Abstract* – Investigation of electrical characteristics of fully-depleted SOI (silicon-on-insulator) and bulk-Si n-MOSFET devices in order to compare their electrical characteristics using SILVACO TCAD software was done and presented in this paper. Two specific channel lengths of the device that had been concentrated are 0.5 and 0.35 micron. The comparisons were focused on three main electrical characteristics that are leakage current, threshold voltage and subthreshold voltage. The device structures were constructed using Silvaco-Athena and the characteristics were examined and simulated using Silvaco-Atlas. Results were analyzed and presented to show that the electrical characteristics of fully-depleted SOI devices are better than bulk-Si devices. It has also shown that the fully-depleted SOI device is superior in the submicron region.**

***Keywords* – Silicon-On-Insulator, MOSFET, Fully-Depleted, SILVACO**

I. INTRODUCTION

Silicon technologies have progressed faster year to year. The main issue must be concentrate about silicon technologies is how much the silicon devices can be scaled down and what is the effect of reducing the dimension of devices [1]. There are many serious problems for standby power consumption of ultra-large-scale integration (ULSI) circuits when having a silicon metal-oxide semiconductor field-effect transistor (MOSFET) that have gate dimension goes down into the deep submicron region. One of the foremost problems to overcome is the source/drain junction formation technique, which avoid short-channel effects for nano-scale devices [2].

To overcome the problem, a new circuit design techniques has been introduce for a newer technologies such as Silicon-on-Insulator (SOI). SOI refers to placing a thin layer of silicon on top of an insulator, usually silicon dioxide (SiO_2) or known as buried oxide layer (BOX). The research and development on SOI technology have been progressed rapidly since 1998 [3].

Insulator thickness or buried oxide layer (BOX) usually in range between 200nm and 500nm [4]. In SOI structures, the active region of substrate is separate from the main silicon substrate in order to reduce the electrical current leakage of the device. Thus, the area of electrically active silicon can increase the switching speeds of the device [5]. Fig. 1 show cross-section of bulk compared to SOI device [6]. The different between these two substrates is the insertion of insulation layer beneath the devices. Because of that, it gives the result of lower parasitic capacitance and makes faster switching and lower power dissipation [7].

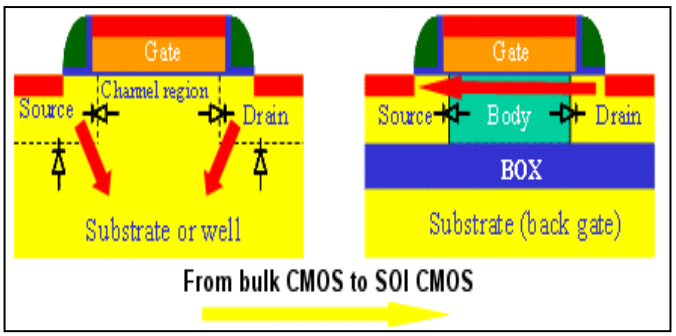


Fig. 1: The structure of bulk-Si and SOI device

The silicon layer thickness typically is from several microns to less than 500 angstrom. MOSFETs fabricated on SOI substrate that having a relatively thin SOI layer is known as fully depleted SOI and for thick SOI layer is known as partially depleted SOI. Usually, for fully-depleted SOI devices, the thickness of silicon is about less than 100nm [5]. The full isolation in SOI device provide many advantages such as the drain-to-substrate capacitance can be neglected due to insulator (SiO_2) that having dielectric constant lower than Silicon [3].

Besides that, SOI can produce lower threshold voltage and steeper subthreshold swing that lower than 60mV/decade and be able to achieve a higher drive current (due to smaller threshold voltage). When the thicknesses of silicon become thinner, it will make the devices more powerful and yield excellent electrical characteristics such as subthreshold swing about 10mV/decade can be achieve and make its suitable for low leakage technology [8]. In SOI technology also, the power consumption may cut nearly by half, with speed improvements 20% to 50% increase in switching speed compared to Bulk-Si devices [4]. Fig. 2 shows the cross section of fully-depleted SOI compared to partially-depleted SOI devices [6]. The key feature of a fully-depleted SOI device is that the depletion region reaches all the way to bottom of the Si film. As a result, the body region is fully depleted, as the name of the device indicates [3].

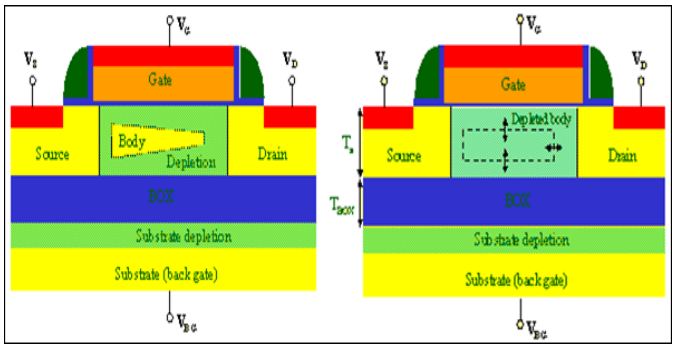


Fig. 2: The structure of partial-depleted SOI and fully-depleted SOI device

II. Objectives

The main objectives of this research are:

1. To investigate the advantages of using SOI in CMOS fabrication compared to bulk CMOS.

2. To study the effect of fully-depleted SOI on leakage current, threshold voltage and subthreshold voltage.

3. To simulate the electrical characteristic of fully-depleted SOI n-MOSFET at 0.35 micron and 0.5 micron of channel length by using SILVACO TCAD software.

III. Methodology

The design process of bulk-Si n-MOSFET and fully-depleted SOI n-MOSFET was done by using SILVACO TCAD software. The structure of the devices was simulated using Silvaco-Athena and for simulating the devices electrical characteristics, Silvaco-Atlas was used to plot the graph and extract its electrical parameters.

A. ATHENA and ATLAS Simulation

ATHENA framework integrates several process simulation modules within a user-friendly environment provided by SILVACO TCAD interactive tools. ATHENA process simulators are used to create the structures of the bulk-Si devices while for fully-depleted SOI devices, ATLAS Syntax was used to create the structures.

In this research, the devices was constructed according to specific recipe and the variable such as temperature, time and impurities dose are varied in order to get acceptable value of electrical parameters. Tonyplot was used to display the structures. To construct the structures, the process involve in ATHENA consist of several step such as diffusion, ion implantation, deposition and etching.

ATLAS is a physically-based two dimensional device simulator. It predicts the electrical behavior of specified semiconductor structures, and provides insight into the internal physical mechanisms associated with device operation. The electrical parameters of the devices that constructed by ATHENA was examined or simulated using ATLAS. The plot of Id-Vg and Id-Vd curves was generated using Tonyplot. From the plot, the electrical parameters value such as threshold voltage, leakage current and subthreshold voltage was extracted in ATLAS. Fig. 3 shows the flow chart of the simulation.

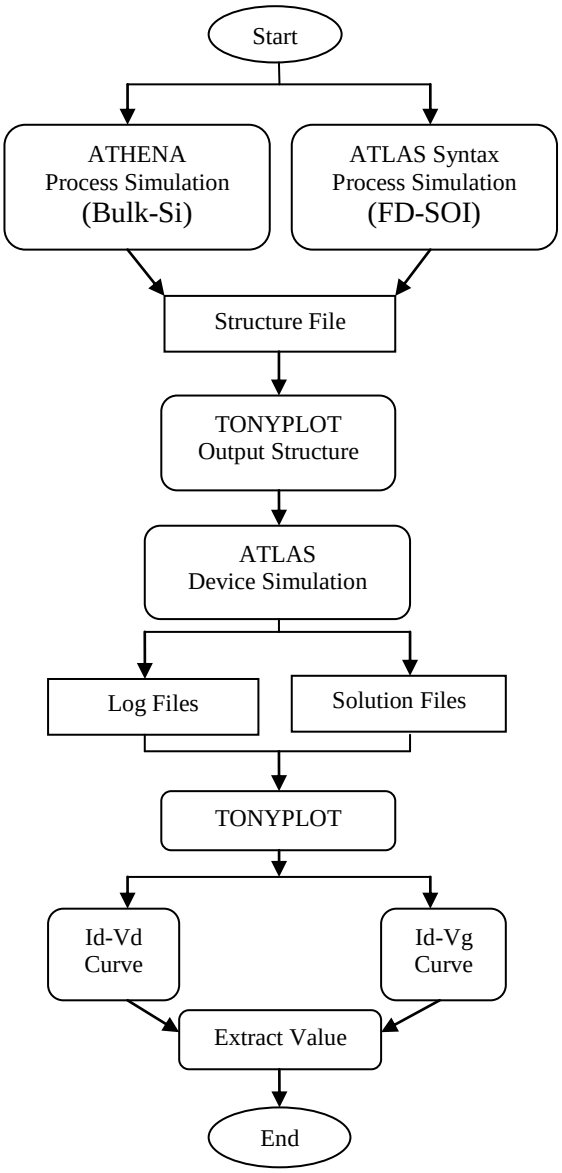


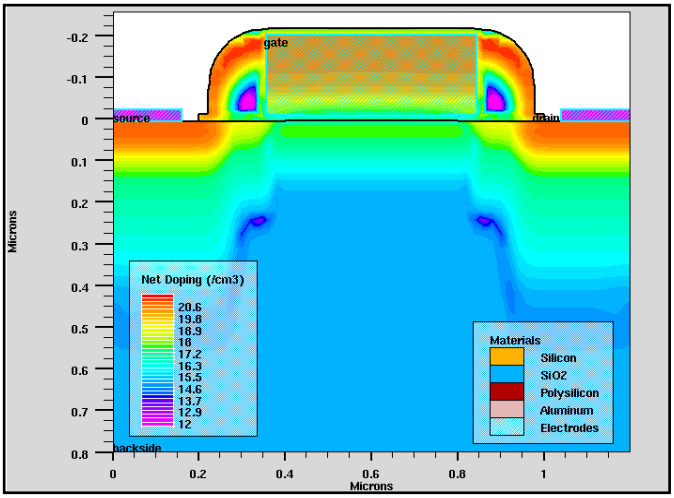
Fig. 3: Simulation flow chart

IV. Result and Discussion

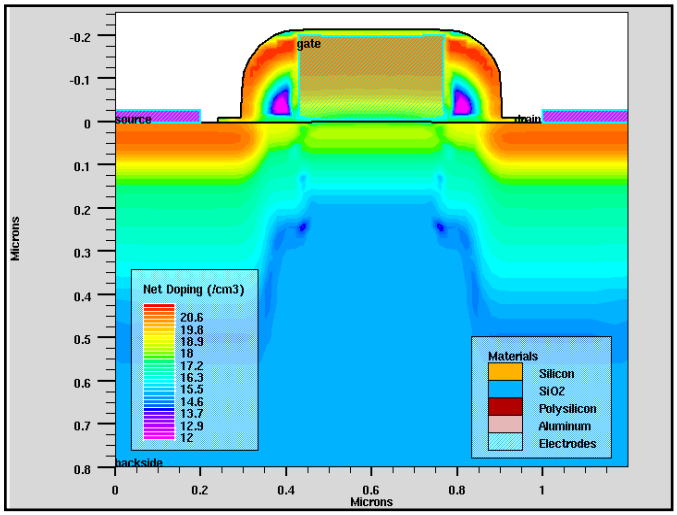
A. Electrical Characteristics of bulk-Si n-MOSFET

Fig. 4 (a) and (b) shows the structures of 0.5 um bulk-Si n-MOSFET and 0.35 um bulk-Si n-MOSFET. The channel length can be observed by looking the length of gate. The channel doping of 0.5 micron structures is $2.2E12cm^{-3}$ that has been doped with boron while for drain and source doping concentration is $5.0E15cm^{-3}$ that has been doped with

arsenic. For the 0.35 micron structure, the channel doping of is 7.5E12cm^{-3} while for drain and source doping concentration is 5.0E15cm^{-3}. The doping concentrations of the structures have been varied in order to get the optimum value that satisfied all three electrical parameters. The structures were display by contour plot menu that can be observed the net doping of structures.



(a)

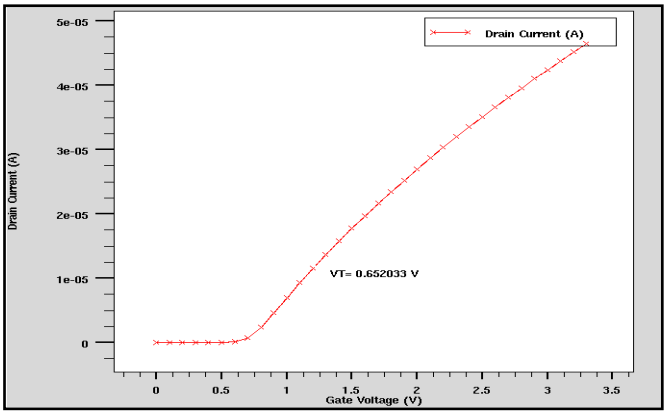


(b)

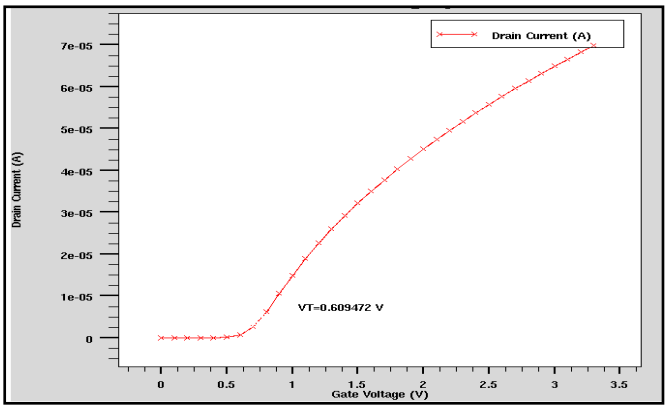
Fig. 4: The Structures of bulk-Si n-MOSFET at different channel length: (a) 0.5 micron (b) 0.35 micron

The plots for the threshold voltage of bulk-Si n-MOSFET at different channel length are shown in fig. 5 (a) and (b). The plots of Id versus Vgs was applied with dc bias of Vds= 0.1 V and ramp the gate voltage from 0 V to 3 V with a bias step size of 0.1 V.

At 0.5 um channel length, the threshold voltage is 0.65 V while for 0.35 um channel length the threshold voltage is 0.61 V. It shows the threshold voltage was decreased as the device size shrinks.



(a)

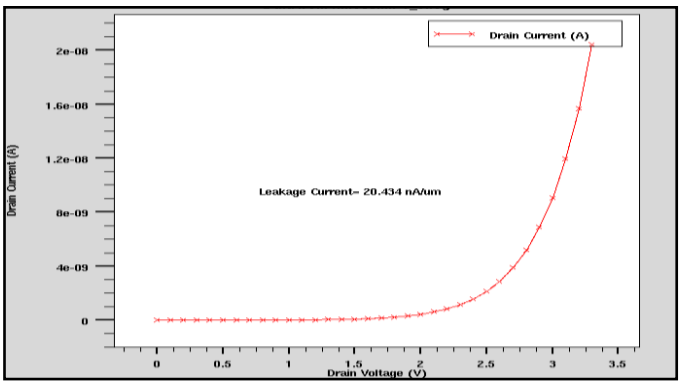


(b)

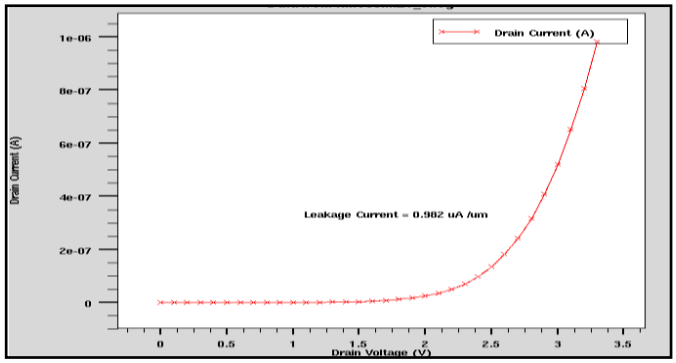
Fig. 5: Threshold voltage of bulk-Si n-MOSFET: (a) 0.5 micron (b) 0.35 micron

The plots for the leakage current of bulk-Si n-MOSFET at different channel length are shown in fig. 6 (a) and (b). The plots of Id versus Vds was applied with dc bias of Vds = 0.1 V and ramp the drain voltage from 0 V to 3.3 V with a bias step size of 0.1 V.

At 0.5 um channel length, the leakage current is 20.43 nA/um while for 0.35 um channel length the leakage current is 0.98 uA/um. It shows the leakage current was increased as the device size shrinks.



(a)

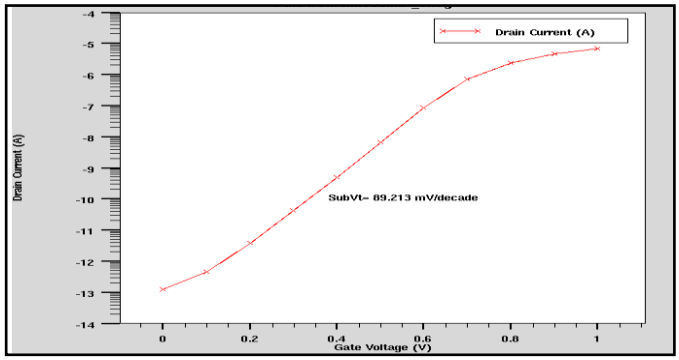


(b)

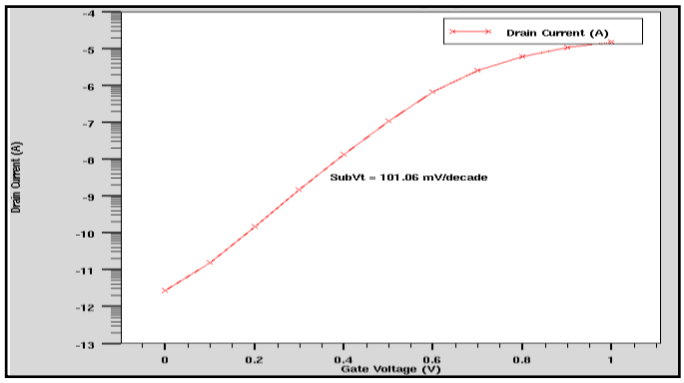
Fig. 6: Leakage current of bulk-Si n-MOSFET: (a) 0.5 micron (b) 0.35 micron

The plots for the subthreshold voltage of bulk-Si n-MOSFET at different channel length are shown in fig. 7 (a) and (b). The plots of log Id versus Vgs with fixed Vds was applied with bias the drain from 0.025 V to 0.1 V with a bias step size of 0.025 V and ramp the gate voltage from 0 V to 0.1 V with a bias step size of 0.1 V.

At 0.5 um channel length, the subthreshold voltage is 89.21 mV/decade while for 0.35 um channel length subthreshold voltage is 101.06 mV/decade. It shows the subthreshold voltage was increased as the device size shrinks.



(a)



(b)

Fig. 7: Subthreshold voltage of bulk-Si n-MOSFET: (a) 0.5 micron (b) 0.35 micron

Table 1 shows the comparison of electrical characteristics of bulk-Si n-MOSFET with different channel length. Its shows the decreasing in the threshold voltage and increasing in subthreshold voltage and leakage current of the n-MOSFET as the device size shrinks.

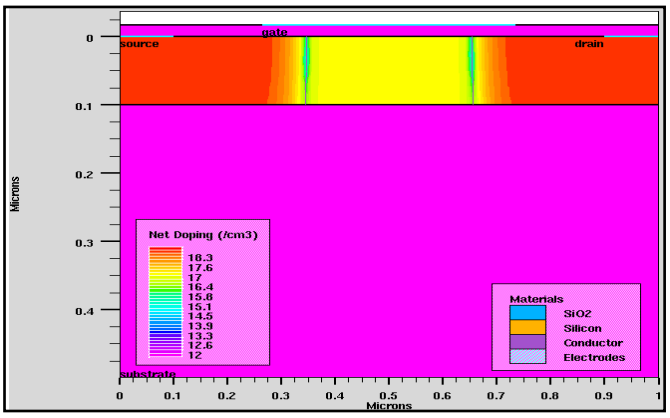
TABLE 1

THE EXTRACTED VALUES OF THE ELECTRICAL CHARACTERISTICS OF BULK-Si n-MOSFET AT DIFFERENT CHANNEL LENGTH

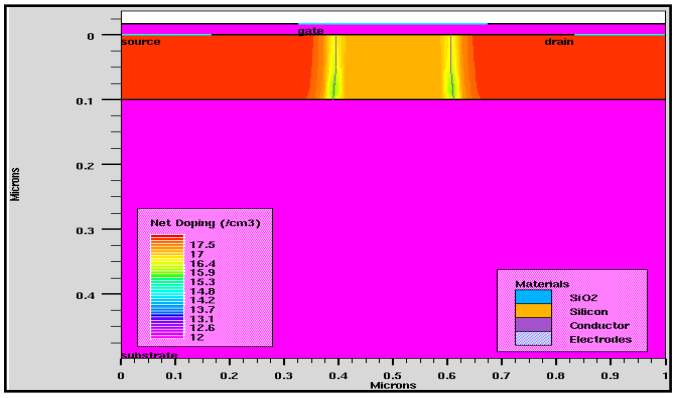
Electrical characteristics	0.5 um	0.35 um
Vth (V)	0.652	0.609
Ids_leakage (A/um)	20.43 n	0.98 u
SubVth (mV/decade)	89.21	101.06

B. Electrical Characteristic of fully-depleted SOI n-MOSFET

Fig. 8 (a) and (b) shows the structures of 0.5 um of fully-depleted SOI n-MOSFET and 0.35 um of fully-depleted SOI n-MOSFET. The channel length can be observed by looking the length of gate. The channel doping of 0.5 micron structures is 1.203E17cm^{-3} that has been doped with p-type material while for drain and source doping concentration is 5.0E18cm^{-3} that has been doped with n-type material. For the 0.35 micron structure, the channel doping of is 1.36E17cm^{-3} while for drain and source doping concentration is 9E17cm^{-3}. The doping concentrations of the structures have been varied in order to get the optimum value that satisfied all three electrical parameters. Both gate oxide thicknesses structures is 17nm and silicon film thicknesses is 100nm while for insulator (BOX) thickness is 400nm. The substrate of the device has not shown on the structure because of no effect due to insulator above it.



(a)

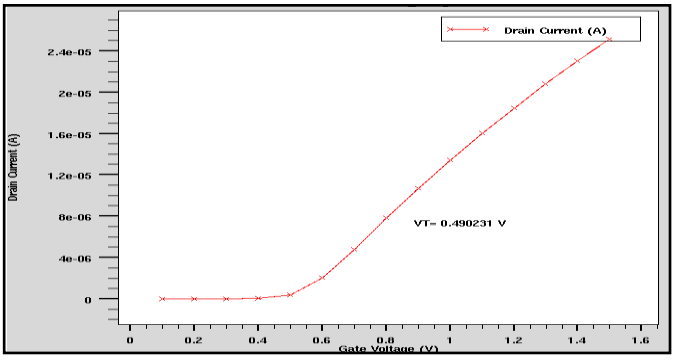


(b)

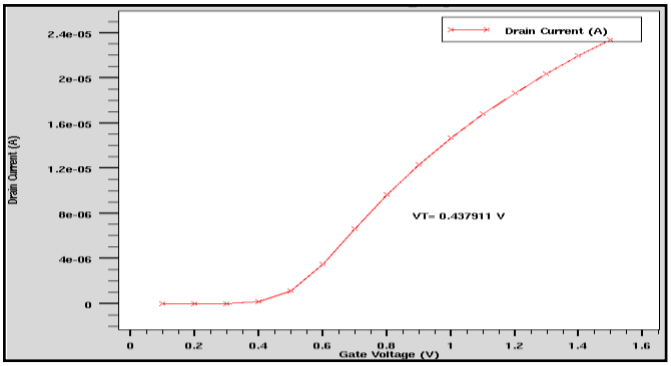
Fig. 8: The Structures of fully-depleted SOI n-MOSFET at different channel length: (a) 0.5 micron (b) 0.35 micron

The plots for the threshold voltage of fully-depleted SOI n-MOSFET at different channel length are shown in fig. 9 (a) and (b). The plots of Id versus Vgs was applied with dc bias of Vds= 0.1 V and ramp the gate voltage from 0.10 V to 1.5 V with a bias step size of 0.1 V.

At 0.5 um channel length, the threshold voltage is 0.49 V while for 0.35 um channel length the threshold voltage is 0.44 V. It shows the threshold voltage of fully-depleted SOI device was decreased as the device size shrinks.



(a)

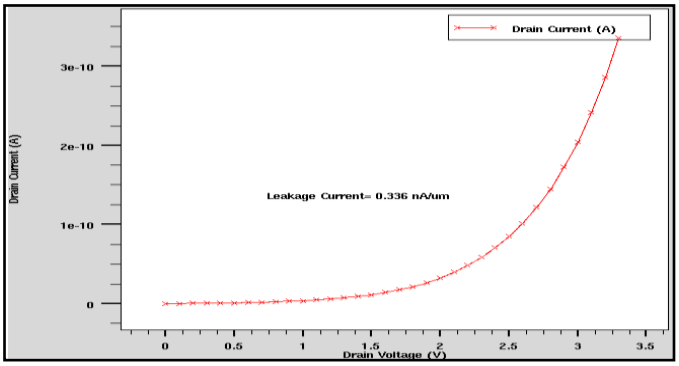


(b)

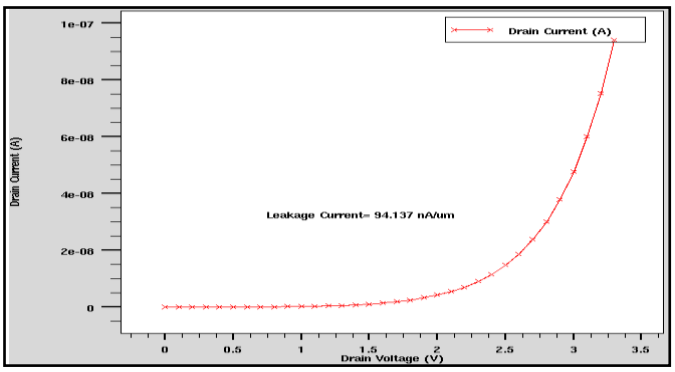
Fig. 9: Threshold voltage of fully-depleted SOI n-MOSFET at different channel length: (a) 0.5 micron (b) 0.35 micron

The plots for the leakage current of fully-depleted SOI n-MOSFET at different channel length are shown in fig. 10 (a) and (b). The plots of Id versus Vds was applied with dc bias of Vds= 0.10 V and ramp the drain voltage from 0 V to 3.3 V with a bias step size of 0.1 V.

At 0.5 um channel length, the leakage current is 0.34 nA/um and for 0.35 um channel length the leakage current is 94.14 nA/um. It shows that the leakage current fully-depleted SOI was increased as the device size shrinks.



(a)

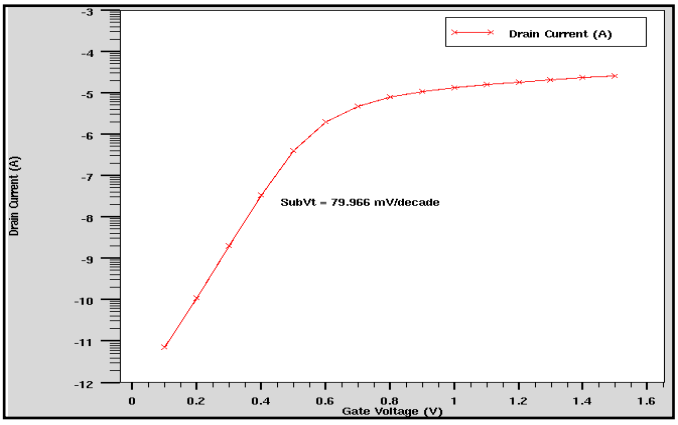


(b)

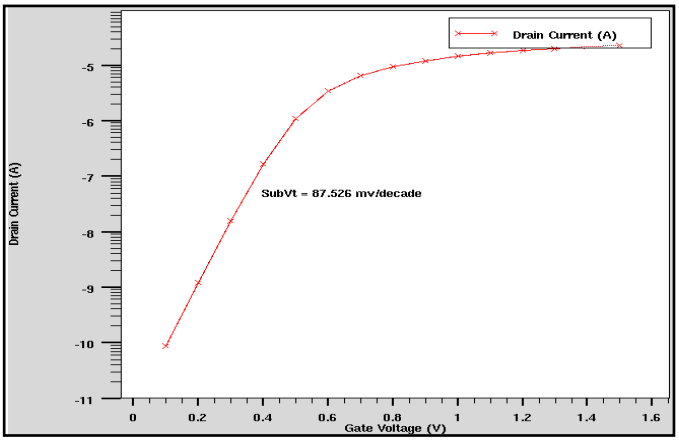
Fig. 10: Leakage current of fully-depleted SOI n-MOSFET at different channel length: (a) 0.5 micron (b) 0.35 micron

The plots for the subthreshold voltage of fully-depleted SOI n-MOSFET at different channel length are shown in fig. 11 (a) and (b). The plots of log Id versus Vgs was applied with fixed Vds at 0.05 V and 0.1 V and ramp the gate voltage from 0.1 V to 1.5 V with a bias step size of 0.1 V.

At 0.5 um channel length, the subthreshold voltage is 79.97 mV/decade while for 0.35 um channel length subthreshold voltage is 87.53 mV/decade. It shows the subthreshold voltage fully-depleted SOI was increased as the device size shrinks.



(a)



(b)

Fig 11: Subthreshold voltage of fully-depleted SOI n-MOSFET at different channel length: (a) 0.5 micron (b) 0.35 micron

Table 2 shows the comparison of electrical characteristics of fully-depleted SOI n-MOSFET with different channel length. Its shows the decreasing in the threshold voltage and increasing in subthreshold voltage and leakage current of the fully-depleted SOI n-MOSFET as the device size shrinks.

TABLE 2

THE EXTRACTED VALUES OF THE ELECTRICAL CHARACTERISTICS OF FULLY-DEPLETED SOI n-MOSFET AT DIFFERENT CHANNEL LENGTH

Electrical characteristics	0.5 um	0.35 um
Vth (V)	0.490	0.438
Ids_leakage (nA/um)	0.34	94.14
SubVth (mV/decade)	79.97	87.53

C. Comparison of Electrical Characteristics

TABLE 3

COMPARISON OF THE ELECTRICAL CHARACTERISTICS BETWEEN FD SOI n-MOSFET WITH BULK-Si n-MOSFET AT 0.5 MICRON

Electrical characteristics	FD SOI	BULK-Si
Vth (V)	0.490	0.652
Ids_leakage (nA/um)	0.34	20.43
SubVth (mV/decade)	79.97	89.21

TABLE 4

COMPARISON OF THE ELECTRICAL CHARACTERISTICS BETWEEN FD SOI n-MOSFET WITH BULK-Si n-MOSFET AT 0.35 MICRON

Electrical characteristics	FD SOI	BULK-Si
Vth (V)	0.438	0.609
Ids_leakage (uA/um)	0.094	0.982
SubVth (mV/decade)	87.53	101.06

Table 3 and 4 shows the comparison of electrical characteristics between fully-depleted SOI n-MOSFET with bulk-Si n-MOSFET. The results show the electrical characteristics of fully-depleted SOI n-MOSFET was better than bulk-Si n-MOSFET. Fully-depleted SOI n-MOSFET has lower threshold voltage compared to bulk-Si n-MOSFET. The SOI device was fully-depleted thus the drain-to-substrate capacitance can be negligible and there is no latch-up occurs. Besides, SOI device have positive body bias of stacked gates because it takes a value between the source and drain biases. These will yield a lower threshold voltage hence improve the switching speed of the devices.

The leakage current of fully-depleted SOI n-MOSFET has smaller than bulk-Si n-MOSFET. This is because the impurities in the n^+ and p^+ regions diffuse deeply into the thin Si film, leaving a p-n junction only at the sidewall of the diffuse area.

Since the body region of fully-depleted SOI devices is fully-depleted, the channel surface potential of fully-depleted SOI ($\emptyset_{SFD}$) devices greater than bulk-Si device that yield the subthreshold slope become steeper. This is due to gate-substrate capacitance in fully-depleted SOI devices is comprised of the series connection of Cox and the body-depletion-layer capacitance (C_B) together with the capacitance (C_{BOX}). This will yield the subthreshold voltage in fully-depleted SOI n-MOSFET become steeper and smaller than bulk-Si n-MOSFET.

According to book title of Fully-Depleted SOI CMOS Circuits and Technology for Ultralow-Power Applications by Takayasu Sakurai, Akira Matsuzawa and Takakuni Douseki, equation (1), (2) and (3) shows the relationship between channel surface potential, gate voltage

and subthreshold swing, S which defined as change in gate voltage needed to change the drain current by one decade in subthreshold region.

$$S = \frac{kT}{q} \ln(10) \Big/ \frac{\partial \emptyset_{SFD}}{\partial V_G} \quad (1)$$

$$\emptyset_{SFD} = \frac{C_{OX}}{C_{OX} + C_{SOI}} \quad (2)$$

Where

$$C_{SOI} = \frac{C_B}{1 + C_B / C_{BOX}} \quad (3)$$

IV. CONCLUSION

The comparison of electrical characteristics of fully-depleted SOI n-MOSFET with bulk-Si n-MOSFET was done successfully. Based on the results obtained, it can be concluded that as compared to bulk-Si devices, fully-depleted SOI devices shows the ability to improve the electrical characteristics such as lower threshold voltage, steeper subthreshold swing and lower leakage current.

These are very important which can reduce the power consumption as much as possible to prolong battery life. Besides that, the speed improvement enables produce much greater system performance. Moreover, major reduction in electrical characteristics compared to bulk-Si devices promise to result in faster and faster chips as development is carried forward into the future. However, when scaling continues in SOI devices, the parasitic effects will also appear increasing the leakage current and subthreshold voltage.

Further research can be implementing on Strain Silicon on Insulator devices which combination between SOI technologies with Strain technologies. The combination between two technologies offers more improvement on current drive, faster switching times, lower power consumption and lower voltage operation.

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