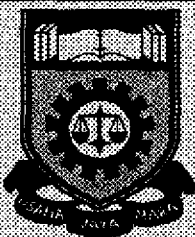


PLD PROGRAMMER USING PC

**This thesis is presented in partial fulfilment for the award of the
Bachelor of Electrical Engineering (Hons.) of
MARA INSTITUTE OF TECHNOLOGY**



**ROSSILAWATI BT ABDUL HAYET
School of Electrical Engineering
MARA Institute of Technology
40450 Shah Alam
MAY 1997**

ABSTRACT

This project explores the hardware and software development for programming of programmable logic ICs. The objective of the project is to design a programmer circuit and develop the software to be able to programme the programmable logic device (PLD) by using personnel computer(PC). In this case EPROM family are selected as a case study. The types of EPROM that has been tested are 27256,27128 and 2764. When the input is given to this circuit, it will be automatically tested using the QBASIC software. Then it will give the result. QBASIC is also used to communicate between the programmer circuit and the PC by using serial data transfer technique.

ACKNOWLEDGMENT

In the name of **ALLAH s.w. t.**, the Beneficent, the Merciful. It is wish the deepest sense of gratitude to **ALLAH** who has given me strength and ability to complete this project and the thesis as it is today.

I would like to express my most appreciation and heartfelt gratitude to **Mr. Ahmad Maliki Omar** as my project supervisor, for his guidance, encouragement and ideas from beginning up to end of my project. My gratitude also goes to all the lecturers who had tough me and technicians, staff at machine laboratory who gave me information, suggestions in improving the project and gave me full cooperations towards success of my project.

I'm also would like to express my special gratitude to my family for their inspiration and invaluable support along the duration of my studies until this thesis is completed. Last but not least, my special thanks to all my friends for their valuables asistance, who help me directly or indirecely in carrying out the work and reached the goal. **THANKS.**

PLD PROGRAMMER USING PC

<u>CONTENTS</u>	Page No.
ABSTRACT	i
ACKNOWLEDGEMENT	ii
CONTENTS	iii
CHAPTER 1	
1.0 INTRODUCTION	
1.1 Overview Of PLD	1
CHAPTER 2	
2.0 SCOPE OF PROJECT	
2.1 The Existing PLD	3
2.2 The New System	4

CHAPTER 1

1.0 INTRODUCTION

1.1 Overview Of PLD

Programmable logic devices (PLDs) are a logic ICs which can be programmed by the user to perform a wide variety of logic functions. A circuit structure in PLDs is usually a rectangular array of identical cells, that can be individually programmed[1].

PLD can be programmed by the user or supplier in the field, either using PROM or EPROM technology. In PROM technology the devices can be used only once. Where EPROM technology is employed the device is erasable and reprogrammable. The machine that is involved to programme the PLDs is called PLD Programmer[2,3].

PLD have four different types. There are PLA(Programmable Logic Array), PAL (Programmable Array Logic), Programmable Logic Element and lastly PGA (Programmable Gate Array). PLA contains a set of AND gates connecting to a set of OR gates. There are selectable link fuse the device inputs into the AND gates and between the AND gates and OR gates so that combinations sum of product expressions can be realized[2].