DESIGN 16 TO 1 MULTIPLEXER USING MENTOR GRAPHICS DESIGN TOOLS

This thesis is presented in partial fulfillment for the award of the

Bachelor of Electrical Engineering (Hons.)

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ACKNOWLEDGEMENT

All praise to God, The Most Beneficent and The Most Merciful. First and foremost, thank to The God Almighty for His bounty and blessing upon us who have give me strength and ability to complete this project report.

I would like to express my appreciation to my supervisor, Puan Hashimah Hashim, for her guidance, invaluable suggestion and comment throughout the project completion. This project would not be accomplished without her encouragement and her constructive critic.

A special thank to my family, especially to my parents Hasan Bin Puteh and
who are dearest person in my life and greater source of inspiration. Thank you for their loves and support in completing this project.

Lastly, I would like to thank all my friends for their invaluable assistance and discussion concerning this project and also to all who have been involved directly or indirectly.

ABSTRACT

The main purpose of this project is to design the 16 to 1 multiplexer layout using Mentor Graphics Design Tools. The main objectives of this project are to design 16 to 1 multiplexer using Mentor Graphics Design software, to produce the output waveform of multiplexer from simulation and design layout to get the 16 to 1 multiplexer chip with application. The design based on basic multiplexer structure which consists of AND, OR and INVERTER CMOS gates. Full custom design flow is implemented in which the design starts with schematic followed by simulation for characterization purpose and validation. The layout of the multiplexer is achieved along with the post layout simulation and layout verification. The designed multiplexer is tested by simulation to determine the functionality and performance.

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CHAPTER 1

INTRODUCTION

1.1 Overview

Integrated circuit design is becoming more complex every day. This is especially true in analog and mixed-signal design. To address critical time-to-market issues as designs become increasingly complex, Mentor Graphics has developed a complete analog/mixed signal IC design flow, from schematic capture to physical layout and verification. This project is one of the integrated circuit design to design of 16 to 1 multiplexer using Mentor Graphics.

Multiplexer used in many building digital semiconductors such as CPUs and graphics controllers. Multiplexers are also used in communications; the telephone network is an example of a very large virtual multiplexer built from many smaller discrete ones.

Many processes have been integrated to produce this device, including: design the schematic diagram, netlist that generated from the schematic testbench, produce the output waveform from the netlist, layout that generate from the schematic diagram, check the layout using DRC and check the layout and schematic using LVS.