

**DIGITAL NEURON INTEGRATED CIRCUIT DESIGN FOR  
FEEDFORWARD NEURAL NETWORK USING SILTERRA  
0.13MICROMETER TECHNOLOGY**

**This thesis is presented in partial fulfilment for the award of the  
Bachelor of Engineering (Hons.) Electronics, Universiti Teknologi Mara Malaysia**



**MOHAMAD FAIZ OMAR BIN MAHMUD  
FACULTY OF ELECTRICAL ENGINEERING  
UNIVERSITI TEKNOLOGI MARA  
40450 SHAH ALAM,  
SELANGOR, MALAYSIA  
JULY 2012**

## **ACKNOWLEDGEMENT**

I would like to extend my gratitude and thankful to my Final Year Project (FYP) supervisor, Dr Wan Fazlida Hanim Abdullah for her concern, guidance, assistance and advise towards the progress of completing my final year project. Throughout a year to finish the final year project, Dr Wan Fazlida Hanim Abdullah has been patiently and continuously advising me in order to get the right direction and offering encouragement. Obviously, my final year project will be uncertain and uncompleted without her assistance and advices. Last but not least, special thanks to all who are participating directly or indirectly during completing my final year project.

## ABSTRACT

Artificial Neural Networks (ANNs) is an interconnected group of neurons that uses a mathematical model for information processing often done using computational method. The neural network faces timing issues because it consists of many gates due to the repetition of neurons. This thesis presents the design and comparison of the neuron architecture between tree and ring structure in terms of functionality, usage of resources, total thermal power dissipation and timing analysis. Then, we perform the analysis of feedforward neural network that consists of several. The objective of the project is to design a neuron on digital platform using hardware description language for their functionality and analysis purpose. The best structure will be implemented as integrated circuit. Neuron layout is designed using custom approach based on schematic from post synthesis done in Quartus II. IC design is designed using Cadence Design Systems Virtuoso targeted for Silterra 0.13 micrometer technology. Since both structures have tradeoffs in their advantages, we decide on the layout ring structure as it more reliable compared to tree in terms of delay. The number of resources usage for tree structure is 423 while the ring structure is 425. The delays of tree and ring structure are 29.047ns and 27.340ns respectively. The performance of neural network is dependent on the performance of neuron. The ring structure of neuron and neural network IC layout has a size of 680 $\mu$ meter x 2493 $\mu$  meter and 3211 $\mu$  x 2351 $\mu$  meter respectively.

*Keywords-component; feedforward; neuron; neural networks;*

## TABLE OF CONTENTS

ACKNOWLEDGEMENT .....	i
ABSTRACT .....	ii
TABLE OF CONTENTS.....	iii
LIST OF FIGURES .....	v
LIST OF TABLES .....	vii
LIST OF SYMBOLS AND ABBREVIATIONS .....	viii
1.0 INTRODUCTION .....	1
1.1 Project Background .....	1
1.2 Problem Statement .....	3
1.3 Objectives.....	4
1.4 Scope of Work.....	6
1.5 Gantt Chart.....	7
2.0 LITERATURE REVIEW .....	8
2.1 Introduction .....	8
2.2 Model of Artificial Neuron .....	10
2.3 Neural Network Implementation Using Verilog and Custom Layout Design: Issues and Application .....	12
2.4 Structure of a Neuron .....	13
2.5 5x5-Bit Baugh Wooley (Array) Multiplier .....	14
2.6 Chapter Conclusion .....	15
3.0 METHODOLOGY .....	16
3.1 Introduction .....	16
3.2 Design Flow Chart .....	16
3.3 Data Flow .....	18

# **CHAPTER 1**

## **INTRODUCTION**

### **1.1 PROJECT BACKGROUND**

A neural network is an artificial representation of the human brains that used learning process as their principle. In other words, it mimics certain processing capabilities of the human brain. Neural computing is an information processing paradigm, inspired by biological system, composed of a large number of highly interconnected processing elements (neurons) working in unison to solve the specific problems. In engineering, it is a computational model that learns by training on past experience using an algorithm which modifies the interconnection weights as directed by a learning objective for a particular application. It consists of repetition of adder and multiplier units with hyperbolic activation functions [1].