FABRICATION AND CHARACTERIZATION OF 130nm NMOS USING SILVACO SOFTWARE

Thesis is present in partial fulfillment for the award of Bachelor (Honors) of Electrical Engineering Universiti Teknologi Mara

MAS FEZAH BINTI LATIB
FACULTY of ELECTRICAL ENGINEERING
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM,
SELANGOR DARUL EHSAN

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Mas Fezah Binti Latib,
Faculty of Electrical Engineering
Universiti Teknologi Mara
Shah Alam
Selangor Darul Ehsan.

ABSTRACT

This paper presents to find the sequence of dominance for factors that determine the performance of a 130nm technology NMOS transistor. Going to 130nm, requires a lot of changes in the fabrication technique. The supply and threshold voltages will have to continually scale to sustain performance increase, limit energy consumption, control power dissipation, and maintain reliability. ATHENA and ATLAS module of SILVACO software are the tools used in simulating the fabrication and also simulating the electrical performance of the transistors. The parameters under investigation were the threshold voltage (V_{TH}) value, I_D-V_D and I_D-V_G relationships. The data produced from the experiments were used to determine the sequence of dominance for the factors involved in the transistor's abovementioned characteristics. From the experimental results, it was shown that the dopant implantation dosage at the source/drain active area contribute the most in determining the V_{TH} value and also for determining the I_D-V_G relationship. This is followed by the dosage for V_{TH} adjustment implantation, the dielectric thickness and lastly the dosage of the halo implantation. However, there is no clear pattern found in determining the I_D-V_D relationship.

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CHAPTER 1

INTRODUCTION

1.1 PERSPECTIVE FOLLOW HISTORY

Over the past decades, the MOSFET has continually been scaled down in size, typical MOSFET channel lengths were once several micrometers, but today's integrated circuits are incorporating MOSFETs with channel lengths of about a tenth of a micrometer. Until the late 1990s, the size reduction resulted in great improvement to MOSFET operation with no deleterious consequences. Historically, the difficulties with decreasing the size of the MOSFET have been associated with the semiconductor device fabrication process. For more than 30 years, the integrated circuit (IC) industry has followed a steady path of constantly shrinking device geometries and increasing chip size. This strategy has been driven by the increased performance that smaller devices make possible and the increased functionality that larger chips provide.

Together, these performance and functionality improvements have resulted in a history of new technology generations every two to three years, commonly referred to as "Moore's Law". Each new generation has approximately doubled logic circuit density and increased performance by about 40% while quadrupling memory capacity.