



UNIVERSITY TECHNOLOGY MARA

**COMPARATIVE STUDY ON DIFFERENT TYPE
OF MULTIPLIER IN VERILOG HDL**

NIK AHMAD AFNAN BIN NIK AZMAN

Thesis submitted in fulfilment of the requirements

for the degree of

Bachelor of Engineering (Hons) Electronic Engineering

Faculty of Electrical Engineering

June 2018

ACKNOWLEDGEMENT

First of all, I would like to gratitude my thankful to God for His blessing and mercy for final year project twho entitles “comparative study on different type of multiplier in Verilog HDL” was completed.

Then, my frist thank I would like to express is to my lecturer Mrs Siti Lailatul Binti Mohd Hassan, for leading many great thins for this project especially in verilog code, test-bench and software programming. Her willingness to teach me is really insprising in giving full commitment to finish the project.

It is not possible to undertake a task such as this verilog code without incucrring enormous debts of gratitude to a great number of people. Although it is impossible to name all whose assitance was gratefully received even by this project was conveyed, nonetheless the direct and indirect contribuutin of several people must be acknowledged.

Last but not least, I would like to express mine sincere to helpful classmates as well for helping in completing the project whether direct or indirect and best acknowledge to my parent for their moral support from home.

ABSTRACT

This thesis presents the comparative study on different type of multiplier in Verilog HDL (Hardware Description Language). Multiplier is one of the most important components in digital design system and embedded applications. This research study on the different type of multiplier on the algorithm, implementation on Verilog and performance analysis. Today researches already creates so many type of multiplier. This paper helps by doing comparative study of some of this multiplier for future reference. Three type of multiplier used in this comparative study, that are Array, Vedic and Wallace with variation of 4-bits and 8-bits. This technical paper deals with design, synthesis and simulation using Quartus Prime 17.0 Lite Edition and Modelsim 10.5b. The performance of the multipliers is based on the report power and area. Quartus Prime 17.0 Lite Edition used to check the wire connectivity in logic and module of the design using RTL (Resistor-Transistor logic) circuit. To check the validity and functionality of the multiplier, Modelsim 10.5b software are used. The same input data is used on each multiplier because it is expected to get the same output. In this study, it shows that the performance of multiplier are depending on it algorithm. The algorithm of multiplier help the design become more better in performance of power and area when the number of bits changed.

TABLE OF CONTENTS

	PAGE
APPROVAL	i
DECLARATION	ii
ACKNOWLEDGMENT	iii
ABSTRACT	iv
TABLE OF CONTENTS	v
LIST OF FIGURES	vii
LIST OF TABLES	viii
LIST OF ABBREVIATIONS	ix
CHAPTER TITLE	
1 INTRODUCTION	1
1.0 INTRODUCTION.....	1
1.1 PROBLEM STATEMENT.....	2
1.2 RESEARCH OBJECTIVE.....	3
1.3 SCOPE OF WORK.....	3
2 LITERATURE REVIEW	4
2.0 INTRODUCTION.....	4
2.1 ARRAY MULTIPLIER.....	4
2.2 URDHAVA TIRYAKBHYAM (VEDIC) MULTIPLIER.....	5
2.3 WALLACE MULTIPLIER.....	6
2.4 PREVIOUS STUDY ON MULTIPLIER.....	7
2.5 HALF-ADDER.....	8
2.6 FULL-ADDER.....	9
3 ALGORITHM	10
3.0 INTRODUCTION.....	10
3.1 ARRAY ALGORITHM.....	10
3.2 URDHAVA TIRYAKBHYAM (VEDIC) ALGORITHM.....	11
3.3 WALLACE ALGORITHM.....	12

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

Multiplier is one of the technology that have high request in Digital Signal Processing (DSP). There are many DSP applications that use multiplier for better performances [1]. As the sophistication of the technology the rate of modifying the multiplier also increased [2][3]. There are many researchers already creating better performance multiplier. Some researchers creating new multiplier by modifying the existing multiplier to increase the performance. Reducing the time delay and power consumption are very essential requirements for many applications.

Computerized multipliers are the most normally utilized segments in any advanced circuit outline. They are quick, dependable and productive segments that are used to actualize any task. Contingent on the course of action of the segments, there are diverse kinds of multipliers accessible. Specific multiplier engineering is picked in view of the application [4].