# SIMULATION OF PLANAR AND FINFET TRANSISTOR MODEL FOR DIGITAL GATE APPLICATION

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# ABSTRACT

In this work, FinFET (dual-gate) transistor is simulated using computer added design (CAD) tools to replace the conventional planar MOSFET. Nowadays planar transistors are no longer clean due to current leakage during on-off switches. Thus, these effects have caused some heat and power issues. FinFET transistors offer superior performance as the device is scaled into the nanometer. Therefore, the ON current was investigated by analyzing the I-V characteristic. Also the gate sizing was investigated and the results have shown the differences in their performances. In addition, the SPICE models of 32 nm were employed for inverter, NAND and NOR gates and the results were verified by DC and AC analysis. The results indicate that FinFET circuits have better performance and produced less leakage when compared to planar MOSFET.

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# CHAPTER 1

# INTRODUCTION

## 1.1 BACKGROUND OF STUDY

Through the past few decades of transistor evolution, the thing that remains the same is the transistor was made planar. According to Moore's law, the number of transistors on an integrated circuit chip doubles every two years. As the increasing number of transistors, the chip makers have to shrink the transistor size to give more powerful PCs and electronic gadgets [1].Generally, CMOS planar transistor consists of source, drain, gate and channel. The channel connects the source and drain while gate placed top off. The transistor mostly was built into a silicon substrate of the microchip [2]. Gates has a thin insulating layer that directly above the channel and protrudes slightly above the flat plane of silicon [2]. As the past few decades, to improve the performance of the transistors the chip makers shrink the device into two-dimensional or planar structure. However, the problem that the chip makers have to face was it is difficult for the transistor to turn off when size is smaller [3]. In other word, it makes the current keep on flowing even the transistor has switched off. Thus, this causes current leakage. Figure 1.1 shows the leakage path during the transistor is switched OFF.