DESIGNING A DIGITAL CLOCK USING VHDL

Project Report is presented in partial fulfillment for the award of the Bachelor of Electrical Engineering (Hons)

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ABSTRACT

This project paper presents the designing a digital clock using VHDL. The VHDL modelling used are behavioural, structural and register transfer language (RTL) modelling. By using this technique it shortens the design process and produced more efficient and effective circuit. The development of digital clock consists of oscillator, multiplexing block, second, minute, hour, cathode converter and decoder. The result is shown by timing diagram.

Keywords – VHDL, behavioral modelling, structural modelling.

TABLE OF CONTENTS

CHAPTER 1

INTRODUCTION

1.1 General

A clock is an important tool for human beings in their daily lives activities, which able to help them in keeping the track of time. The most commonly used clock types are analogue clock and digital clock. Nowadays, in the new age of era the digital clock is widely used all over the world. It is easier to fabricate and maintain. Therefore, this project can fulfil the needs of keeping time informed.

This project is designing a digital clock using VHDL. VHDL is stand for (Very High Speed Integrated Circuit) Hardware Description language. It has been extensively used in industry since it was launched by the Gateway in 1983 [1],[2]. Today it becomes one of the very useful and powerful tools in nowadays technology in designing. It is much welcomed and become popular as it able to provide a set of construct that can be applied at multiple levels of abstraction and multiple views of the system. In addition, by using this tool the component used in the digital circuit designed can be reduce therefore the complexity of the circuit can be reduced too.

VHDL code can be modeled either by using the design wizard or typing the model in an empty document by using the text editor. Although this language looks similar as conventional programming languages, there are some important differences. A hardware description language is inherently parallel, i.e. commands, which correspond to logic gates are executed in parallel as soon as a new input arrived [5].