FAILURE MECHANISM OF SILICON GERMANIUM (SiGe) TECHNOLOGY ON 90nm PMOS

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ABSTRACT

This research was conducted to study the effect of strain silicon on 90nm PMOS using graded silicon germanium (SiGe). By introducing graded silicon germanium layer under the gate oxide, the performance of conventional 90nm PMOS and 90nm PMOS with silicon germanium layer was compared. The analysis focused on Id-Vg, Id-Vd characteristic, and hole mobility changes. TCAD SILVACO simulator was used to simulate the device process and electrical characteristic of 90nm PMOS structure. The final result shows that, biaxial strain silicon decreased the drive current on 90nm PMOS structure to 35% observed from test gate voltage of -0.5V. The results were obtained from ATHENA and ATLAS simulator.

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CHAPTER 1

INTRODUCTION

1.1 OVERVIEW

Semiconductor industry has experience the rapid revolution of increasing density transistors in a single chip. This revolution is leading by the scaling of the channel length and this scaling rate still obeying the Moore's Law. While the prediction is the rule of following trends for future development, lot of novel technology being implant to the MOSFET (Metal-Oxide-Semiconductor Field Effect Transistor) to sustain its reliability. One of those novel technologies is SiGe on CMOS construction. It is known in decade that SiGe will increase the drive current of MOSFET caused of the characteristic of that material. In this thesis the issues in enhancing the performance of MOSFET will be discussed.

1.1.1 History of MOSFET

Over the past 40 years, a lot of effort studying the electrical and performance of semiconductors has been done and still continued. Since then, much innovation in scaling the transistors which has led to the present day MOSFETs. The density of transistors increases double in 2 years according to the Dr Gordon Moore that is known as Moore's Law. Moore's law is possible because the transistor size decreases exponentially over time. Moore pointed out that reduced cost per function is the driving force behind the exponential increase in transistor density. It is the exponential reduction in cost per function that drives microprocessor performance and growth of the information technology and semiconductor industry. Figure 1.1 shows the historical feature size reduction during the past three decades and the start of the nanotechnology era for the microelectronic industry as feature size moves from deep submicrometer to nanometer scale.