DESIGN OF CMOS OUTPUT STAGE FOR TELESCOPIC AMPLIFIER

This project is presented in partial fulfillment for the award of the Bachelor of Electrical Engineering (Hons)

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ABSTRACT

This thesis presents a design of a CMOS Output Stage circuit for a Telescopic Amplifier based on the data specifications. The supply voltage is around ±3V with capacitance load equal to 10pF. The open loop gain, phase margin, power dissipation, slew rate also presented based on 0.8 μm technology. The large-signal and small-signal analysis have been done to determine the circuit performance. Both the theoretical calculations and CAD tool simulation are used to compare the result and verify the design. The parameter such as DC voltage gain, power dissipation and unity-gain bandwidth show the results of simulation are greater the calculations and met the requirement. By comparing the results for all the parameter between the hand calculations and simulation method, it shows that the simulation give the best result because almost this results are constant within the range of specification. Finally, the simulation and the performance of the CMOS Output Stage for Telescopic Amplifier are obtained. This project has been successfully done and it can be improved for future development.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

Nowadays, an operational amplifier (op-amp) has become the most important and versatile into virtually every area of analog and mixed analog-digital electronics system design. Op-amps is an analog system that always in a different level of complexity that is used to realize functions ranging from dc bias generation to high speed amplification or filtering.

In general, an operational amplifier is consisting of a five blocks as shown in Figure 1.1-1:

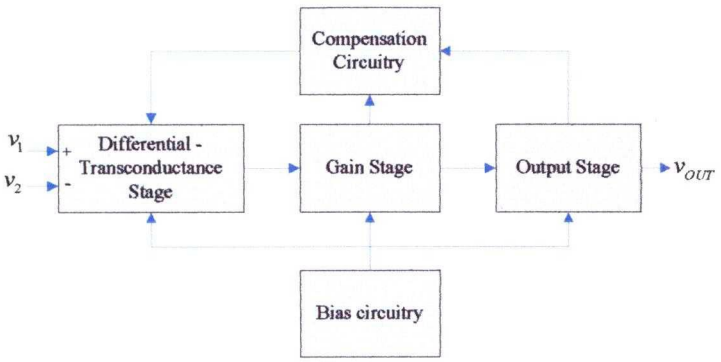

Figure 1.1-1: General block diagram of an Operational Amplifier [1]

The differential transconductance stage forms the input of the op-amp and sometimes provides the differential to single-ended conversion. Normally a good portion of the overall gain is provided by the differential-input stage. The second stage is typically an inverter which is the basic gain stage for Complementary metal-oxide semiconductor (CMOS) circuits before the signal is fed to the output stage. The primary objective of an output stage is to drive an external load without deteriorating the