A COLUMN DECODER and COLUMN DRIVER Used For 2KB SRAM MEMORY

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ABSTRACT

This paper presents A Column decoder and Column driver used for 2KB content addressable SRAM memory. The objective of this paper is to design and analyzed the propagation delay, power consumption, total current consumption and the noise margin. Another objective of this paper is to identify which gates that will be used to design the architecture of Column Decoder. The decoders are controlled by a clock because the SRAM is synchronous. The positive edge of a clock will allow the address to be read into the decoders, both row and column, and enable the correct wordline and bitline. The Column decoder controls multiplexer in the column circuitry to select 2^m bits from the row as the data to access. This designed is used SILVACO EDA Tools software; Gateway simulation for schematic analysis and Expert simulation for designing the layout with 0.18um Silterra technology library. The designed is started with analyzed NAND and NOR gates in term of speed consideration. The NAND gates were gave better propagation delay rather than the NOR gates. Then, NAND gates were improved using a Pseudo NMOS NAND gates. It was gave better propagation delay than NAND gates. A 4 to 16 Column Decoder was implemented of Pseudo NMOS NAND gate for better output. The large Inverter Chain was used as 4 to 16 decoder column driver. Three inverters inside the inverter chain were proved that the driver can drive a large load of capacitance to overcome the problem of speed and power. A full layout of 4 to 16 Column decoder and Column Driver is designed, the design rule check (DRC) is checked with no errors and layout versus schematic (LVS) is equivalent. Overall objective is achieved, Pseudo Nmos NAND gates is used in design the decoder and met the requirement in term of propagation delay, speed, noise margin and reduce the number of area in layout design.

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CHAPTER 1

INTRODUCTION

1.0 Background of Study

Static RAMs use a memory cell with internal feedback that retains its value as long as power is applied. It has the following attractive properties which are denser than flip flops, compatible with standard CMOS process, faster than DRAM and easier to use than DRAM.[1] SRAMs are widely used in applications from caches to register files to tables to scratchpad buffers. The SRAM consists of an array of memory cells along with the row and column circuitry. Figure 1.0 below is the architecture of the SRAM.

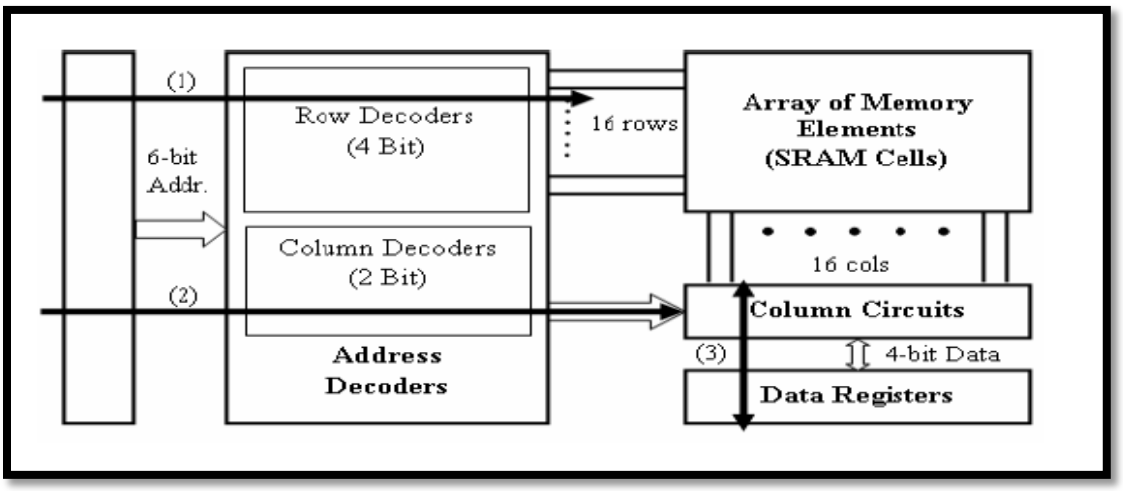

Figure 1.0 SRAM overview