DEVELOPMENT OF DIGITAL CMOS RING OSCILLATOR INTEGRATED CIRCUIT DESIGN

By

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ABSTRACT

This thesis presents the design of a digital Complementary Metal Oxide Semiconductor (CMOS) technology process of ring oscillator circuit. Full custom design flow is implemented in which the design starts with schematic entry followed by simulation for characterization purpose and validation. The IC layout of the ring oscillator is achieved along with the post layout simulation and layout verification. The designed ring oscillator is simulated to determine the functionality and performance.

The design is using 0.5um CMOS technology by MIMOS Berhad and consists of five types of design. Furthermore, the MOSFETs' W/L factor of the ring oscillator circuit also contributes to the characteristics improvement. Different value of MOSFETs widths affected the performance of delay and also noise margin.

The important characteristic of ring oscillator circuit is delay and oscillation frequency. For future development, I have to develop the smaller number of delay with considering MOSFET's W/L in order to get the faster performance of ring oscillator.

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1.1 INTRODUCTION

Ring oscillators are commonly used in measuring delays in various circuits as well as other applications including an internally generated clock source or as a stage in complex systems such as Voltage Controlled Oscillator (VCO) or Phase Locked Loop (PLL). In order to drive a CMOS inverter, the value of N must be an odd number; otherwise a latch forms and hangs at either high or low. As a result of having an odd number of inverters, the ring oscillator does not contain a stable operating point and thus oscillates, making it the ideal circuit for measuring delays.

The issue that must be considered when simulating ring oscillator is necessary to manually start the oscillation. It is because a ring oscillator circuit does not have a stable operating point and the circuit does not drift away from an equilibrium point unless it is perturbed. So, a better approach for designing this circuit is used an initial condition to set on of the nodes in the ring to either ground or to the supply voltage. The actual value used for the initial condition is not very important as long as it is in the normal operating range and it is sufficiently far from equilibrium point. In addition, using initial condition has the advantage of not adding any new components to the circuit.

The consideration taking for designed this circuit is the delay after simulation and after layout. It must follow the specification of MIMOS technology in order to make it operate successfully. The five types of design are tested and simulated using H-SPICE and layout using Tanner EDA.

In order to analyses the circuit performance of CMOS ring oscillator , this term's of thesis explores creating schematics and layouts of inverters, ring oscillators, and test circuit as well as simulating transient responses of the test circuit with respect to the