CLOCK GATING TECHNIQUES USING 0.18µm CMOS TECHNOLOGY

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UNIVERSITI TEKNOLOGI MARA

MUHAMMAD SYAFIQ BIN AB RAHIM
FACULTY OF ELECTRICAL ENGINEERING
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM SELANGOR
MALAYSIA
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ABSTRACT

This thesis presents a study of clock gating techniques using 0.18um CMOS technology. The objective of this paper is to study the speed of the clock gating technique. Another objective of this paper is to study the power consumption of the clock gating technique. Today's consumer demands more functionality, energy efficient device and optimized power device. In order to optimize power of a device the simplest control technique is to shut off the clock of the sequential block of the device when there is no function required from that section for some duration. In synchronous digital circuit the clock net is responsible for significant part of power dissipation (up to 40%) [1]. Clock gating is the most common technique used for optimization and improving efficiency but still it leaves one question how efficiently design is clock gated [2].The simulation results are derived using SILVACO EDA tool, the schematic design and simulation are using the Gateway SILVACO EDA tool. The results show that the AND gate clock gating technique give overall better performance with 299.57ps for the propagation delay, 470.19pW power dissipation and average power of 0.002511W.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

This thesis presents the study of clock gating techniques. There are several techniques of clock gating that can be used. The purpose of this project is to design the clock gating techniques by using 0.18µm CMOS technology. The main design consideration was the speed and power consumption of the clock gating techniques and also to determine which technique can give high speed and low power consumption.

1.2 BACKGROUND OF STUDY

Today's consumer demands more functionality, energy efficient device and optimized power device. In order to optimize power of a device the simplest control technique is to shut off the clock of the sequential block of the device when there is no function required from that section for some duration.

In synchronous digital circuit the clock net is responsible for significant part of power dissipation (up to 40%) [1].The challenge of improving power by adding clock gating is knowing where and when to insert clock gating. Clock gating is the most common technique used for optimization and improving efficiency but still it leaves one question how efficiently design is clock gated [2].