

IMPLEMENTATION OF DCT WITH XILINX VIRTEX

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MUHAMAD RIDZUAN BIN HASHIM
Faculty of Electrical Engineering
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM
SELANGOR, MALAYSIA

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ABSTRACT

This project is about the implementation of DCT with Xilinx Virtex. Xilinx Virtex is used to simulate and implement the Discrete Cosine Transform (DCT) circuit. The outcome of this project will be the process to show how an image from sender will be compressed into pixel values into DCT values. Then it will be changed from pixel values into image to the receiver in a network. This phenomenon is much related to using the software Xilinx ISE 9.2i to implement the DCT. The process will involve synthesizing, analyzing, and studying the DCT to simulate and compare it with the MATLAB simulation using the Xilinx Virtex FPGA program.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The Discrete Cosine Transform (DCT) is a Fourier-related transform using only real numbers. It has roughly twice the length, operating on real data with even symmetry compared with Discrete Fourier Transform (DFT), (since the Fourier transform of a real and even function is real and even), where in some variants the input and/or output data are shifted by half a sample.

In application of image storage or transmission, there is usually a very large amount of image data to be processed. For example, one frame of 512x512 pixel monochrome image at 8 bit/pixel has roughly 2M bit of data. The image compression algorithms, which transfer the data into different domains or encode the data into the proper coding system, are able to reduce the redundancy of the raw image. Discrete Cosine Transform (DCT) is an image compression technique, which is effective to compress a wide variety of images by transferring data into frequency domain [1].

The project uses two methods which are MATLAB and Xilinx ISE 9.2i as the primary platform. In the MATLAB application, the objective is to determine the pixel values of the sample image to obtain DCT values. The step involves reading image file, converting RGB image into gray scale, reading the pixel value, computing 2D DCT. The pixel value that was obtained on MATLAB is used as the input for the simulation in Xilinx ISE application. The simulation of DCT in Xilinx ISE environment involves the DCT algorithm that is coded in VHDL. The pixel value is then applied to the testbench waveform to observe the output.