

# **DESIGN OF A GMSK DEMODULATOR**

**Thesis presented in partial fulfilment for the award of the  
Advanced Diploma in Electrical Engineering of  
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**AZIAN BINTI AHMAD**  
Department of Electrical Engineering  
**MARA INSTITUTE OF TECHNOLOGY**  
40450 Shah Alam, Malaysia  
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## **ABSTRACT**

The objective of this project is to study, design and circuit implementation of the Gaussian Minimum Shift Keying (GMSK) demodulator. The demodulator designed is of the coherent type that uses PLL in the clock and carrier recovery circuits which generate the clock signal. The purpose is to remove the intelligence-bearing signal from a modulated carrier and to reconstitute the signal that performed the modulation.

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# CHAPTER 1

## 1.0 INTRODUCTION

Since the current telecommunications network is becoming more digital, a great deal of interest in digital modulation for cellular system has been developed. Digital cellular systems can offer several important advantages including better spectral efficiency, more consistent speech quality and more flexible service. The digital mobile radio communications system will provide high secure voice and / or high speed data transmission.

Digital cellular technology was introduced in 1991 [1]. There are three standards, the Pan - European Global System for Mobile Communication (GSM) System specified by European Telecom Standard Institute (ETSI), the IS-54 American Digital Cellular (ADC) specified by Telecommunication Industry Association (TIA) and the Japanese Digital cellular (JDC) specified by the Ministry of Post and Telegraph (MPT).

In Europe, GSM standard has been chosen as the unified Pan - European basis for the digital cellular system of the 1990's. It allows the roaming throughout Europe. GSM standard operates in 900MHz band. In GSM there are 8 voice channels on one 200kHz radio carrier (full rate) and it will introduce 16 voice channels by the use of half rate speech codecs in near future.