DESIGN A COMPARATOR OF 8-BIT ANALOGUE-TO-DIGITAL CONVERTER (ADC) IN A 0.35µm CMOS TECHNOLOGY BY USING MENTOR GRAPHICS

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ABSTRACT

This thesis present the design of a high performance on-chip comparator of 8-bit Analogue-To-Digital Converter (ADC) has been designed in a 0.35µm Complementary Metal Oxide Semiconductor (CMOS) Technology process. Full custom design flow is implemented in which the design starts with schematic entry followed by simulation for characterization purpose and validation. The IC layout of the comparator is achieved along with the post layout simulation and layout verification. The designed comparator is tested in an 8-bit ADC by simulation to determine the functionality and performance.

The comparator can handle positive and negative input signals. A polarity signal changes the polarity of the threshold level and makes the output signal always active high. The design is based on basic comparator architecture which consists of three stage; pre-amplifier, positive feedback decision circuit and output buffer. This architecture provides both good gain and offset characteristics by combining the pre-amplifier and the positive feedback decision circuit. The MOSFETs' W/L factor of the comparator circuit also contributes to the characteristics improvement. Increment of the pre-amplifier's input MOSFETs widths increases the gain of the comparator while the width of MOSFETs in decision circuit will determine the offset of the comparator.

The results that were obtained through these simulations showed that comparator design achieved power consumption of 958.69µW, with supply voltage of 5V. Further research on the MOSFETs W/L factor has successfully improved the characteristics of the comparator to perform at gain of 7147 dB and the offset of 620µV. The uses of a latch as the positive feedback decision circuit and the improvement in offset have contributed to the speed performance of the comparator to achieve propagation delay of 3.52ns.

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INTRODUCTION

1.1. Introduction

The Analog-To-Digital Converter (ADC) is an essential building block in many digital signal-processing systems. It provides a link between the digital signal-processing systems. It provides a link between the digital signal processor and the analog signals of a transducer. The ADC is considered to be an encoding device, where it converts an analog sample into digital quantity with a prescribed number of bits.

Numerous types of ADCs have been designed for a wide variety of applications. The type of the application largely determines the choice of the ADC conversion technique. From the viewpoint of the implementation, ADCs typically contain one or more comparators, switches, passive precision components, a precise voltage reference and digital control logic.

A good ADC requires a high-performance comparator since the comparator will determine the accuracy of the ADC conversion. There are many circuit configurations of comparators for different applications with different characteristics. Although the basic op-amp configuration can be used as a voltage comparator, in some less demanding low-frequency or speed applications, op-amp will not be considered as a comparator.

In ADC, the gain and offset of a comparator will also contribute to the comparator speed improvement [1]. Hence, it is important to have a comparator with very good characteristics without consuming large amounts of power. The best approach to achieve such requirements is to employ an architecture which contains a preamplifier stage, positive feedback stage and output buffer stage. By