# ZERO CROSS DETECTOR DESIGN USING SINGLE SUPPLY CMOS OPERATIONAL AMPPLIFIER

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## ABSTRACT

The purpose of this project is to explore various circuit techniques in developing the low voltage CMOS analog building blocks such as operational amplifiers. The main objective of these project is to design of high gain, low power and fully differential operational amplifiers with proper compensation techniques. All the designs had been done Using Tanner EDA with 0.25 μm technology. Circuits were aimed to operate standard supply voltage (3V).Achievement of high gain around 80 dB and 45 degree phase margin for stable closed loop operations were the goal of primary concern. The operational amplifier then was applied on zero crossing detectors circuit. Designing, simulation and comparisons of various performance parameters had been done. Simulation had been carried out using SPICE simulator. Layout had been made using Tanner layout editor (L-edit). All kind of analysis including transient, AC, noise has been done.



**Key terms:**

CMOS, operational amplifiers, compensation, phase margin, Tanner.

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# CHAPTER 1

# INTRODUCTION

## 1.1 Background

Operational Amplifiers are one of the most widely used for analog systems. They are employed from dc bias applications to high speed amplifiers and filters. General purpose op amps can be used as buffers, summers, integrators, differentiators, comparators, negative impedance converters, zero cross detector and many other applications. With the quick improvements of computer aided design (CAD) tools, advancements of semiconductor modeling, steady miniaturization of transistor scaling, and the progress of fabrication processes, the integrated circuit market is growing rapidly. Nowadays, complementary metal-oxide semiconductor (CMOS) technology has become dominant over bipolar technology for analog circuit design due to the industry trend of applying standard process technologies to implement analog circuits in chip. There has been a recent trend of placing digital or analog components on the IC chip for various applications.

The development of analog circuits requires both a complete understanding of basic circuit design techniques and knowledge of transistor non-ideality effects on circuit performance. One severe effect comes from device imperfections and random variations in the fabrication process. Despite the technological advances in the fabrication process steps associated with scaled-down feature sizes, the fluctuations in each step that affects the device performances have not scaled down in proportion. The fabrication process is not easily characterized because these variations are random in nature. Such variations could ultimately be a limiting factor on how low the supply voltage, and how reliable sub-micron designs, could be. In order to produce manufacturable analog integrated circuits with high functional yield and a high degree of reliability, the design of such circuits must be robust with respect to random process and device parameter variations (Michael and Ismail, 1993). With the given design criteria, to obtain a compact, low voltage, power-