OPTIMIZATION OF INITIALIZATION MODULE OF DNA SEQUENCE ALIGNMENT ACCELERATOR

Project report presented in the partial fulfillment for the award of the Bachelor of Electrical Engineering (Hons.)

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ABSTRACT

This report presents the development, implementation and optimization of the initialization module of the DNA sequence alignment accelerator. The scopes of this report is focus on the memory reduction and speed optimization on the initialization module using parallelism and divide and conquer methodologies. The development of the optimization using data compression technique is presented in this paper. In this project, the development target is Xilinx Spartan 3E FPGA using 50 MHz oscillator clock. The code is written in Verilog HDL using Xilinx ISE 10.1 and simulation test bench developed using Xilinx ISE 10.1 simulation tool. Theoretical analysis and simulation results have been compared in this paper.

2

TABLE OF CONTENTS

CHAPTER

LIST OF TITLE

PAGE

ACKNOWLEDGEMENTIIABSTRACTIFTABLE OF CONTENTSVLIST OF FIGURESV	DECLARATION	Ι
ABSTRACT F TABLE OF CONTENTS V LIST OF FIGURES V	DEDICATION	п
TABLE OF CONTENTSLIST OF FIGURESVI	ACKNOWLEDGEMENT	III
LIST OF FIGURES V	ABSTRACT	IV
	TABLE OF CONTENTS	v
LIST OF TABLES	LIST OF FIGURES	VIII
	LIST OF TABLES	İX

1.0 INTRODUCTION

1.1	INTRODUCTION	1
1.2	PROBLEM STATEMENT	2
1.3	PROJECT OBJECTIVE	3

2.0 LITERATURE REVIEW

ŝ

2.1	INTRO	ODUCTION	4
2.2	DNA SEQUENCE ALIGNMENT		
2.3	LOCA	L ALIGNMENT	5
	2.3.1	SMITH-WATERMAN ALGORITHM	6
	2.3.2	BLAST	8
	2.3.3	FASTA	9

2.4GLOBAL ALIGNMENTS112.4.1NEEDLEMAN-WUNSCH ALGORITHM12

CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

The demand of fast and less memory usage of DNA sequence alignment accelerator tools for DNA sequences alignment for investigation and analysis study is increasing dramatically time by time. Faster device are demanded by the market nowadays as human beings want the works complete in short period of time. DNA sequence alignment accelerator can be use in pharmaceutical industry, crime investigation department and any other field to increase the completion time.

The genomic database has increase double in every 16 months. The statements supported and proved by the state in [1]. Genomic database will be increase each day and in the future there will be more memory are needed. The phenomenon is supports this project proposal to produce a high speed and performance as the data of genetic increase significantly.

Initialization module developed to prepare the data for the other next module such Matrix filling. This development of initialization module of DNA sequence alignment accelerator can optimize the speed and reduce the memory consumption using parallel architectures and data compression technique. This will fulfill the market that need device with optimized speed and less memory.