# CMOS LOW NOISE OPERATIONAL AMPLIFIER DESIGN

This project is presented in partial fulfillment for the award of Bachelor of Electrical Engineering (Honours) Universiti Teknologi MARA

SAIFUL IZUAN BIN RAMLI
Faculty of Electrical Engineering
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM SELANGOR

# ACKNOWLEDGEMENT

Bismillahirrahmanirrahim and Alhamdulillah,

Firstly, I would like to express my greatest appreciation to my supervisor, Mrs Suhana Sulaiman, a lecturer of Faculty Electrical Engineering, University Technology Mara, for her valuable guidance, constructive comments, advice and continuous encouragement during the entire course of this project.

Secondly, I wish to express my gratitude to all lectures, thank you for your support, which has been a constant source of strength, provide useful advices and moral supports to me.

Finally, I acknowledge with honour my loving parents, Ramli Bin Mohd Tahir, and for their immense motivation and inspiration. Last but not least, to all my friends, Bachelor of Electrical Engineering, thanks for their endless support and advice. I hope that all the knowledge of this project would be useful for others in the future.

Wassalam…

# ABSTRACT

This project is to design a low noise CMOS operational amplifier following on given specification such as Vdd equal to+2.5V, Vss equal -2.5V, capacitance load equal to 5pF, and PMOS input differential amplifier. Some calculations have been done to determine the W/L of the CMOS transistor to obtain the result of the specifications based on generic 0.25μ technology. The noise of the two different topology circuits is compared to prove the low noise result. CAD tools are used to simulate and verify the design. Finally, the schematic and the layout of the CMOS low noise op amp are obtained.

# TABLE OF CONTENTS

# CHAPTER 1

# INTRODUCTION

## 1.1 Introduction

Op-amp is the one of the most versatile and important building blocks in analog circuit design. Basically an operational amplifier is consisting of two stages as shown in Figure 1.1-1:

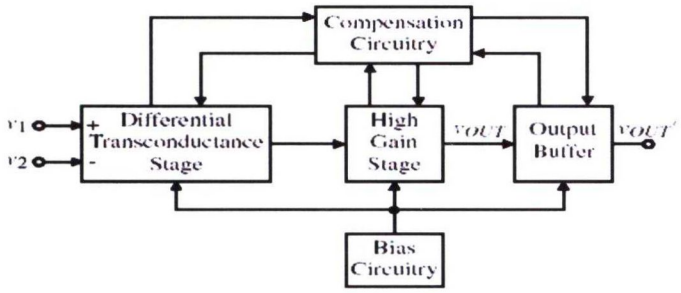


Figure 1.1-1: Simplified model for a two stage operational amplifier [1].

In Figure 1.1-1 there are three different building blocks stage in op-amp. Two gain stages and a unity gain output stage [1]. The first stage is differential amplifier which forms the input and sometimes provides the differential input to single ended conversion [1]. The second stage provides the voltage gain required by the op-amp together with the input stage. Finally, the third stage provides current gain and low output impedance. The output buffer is normally present when resistive load is needed to be driven [1]. The capacitor is included in order to ensure stability when the op amp is used with feedback [1]. Good low noise performance requires maximum gain in the front stages. Therefore differential amplifier is used in order to form high gain.

In this project, low noise CMOS amplifier is designed using tanner software. The design is based on the idea which considers the circuit topology and transistor selection [1]. The one principle that is important in minimizing noise is to make the first stage gain as high as possible. This means that the input differential amplifier source coupled