8-BIT SUCCESSIVE APPROXIMATION REGISTER ANALOG-TO-DIGITAL (SAR ADC) LOGIC DESIGN

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ABSTRACT

This thesis presents the design of a 8-bit Successive Approximation Register (SAR) logic of SAR ADC in a HP 0.5μm SCN3M Complementary Metal Oxide Semiconductor (CMOS). The architecture of SAR logic consists of 3 modules which are shift register, register low-to-high and code register. From this architecture, the performance specification in terms of power consumption, resolution and speed are measured.

The architecture is implemented by using the full custom design approaches. The design starts with the schematic entry followed by simulation for characterization purpose and validation.

The power consumption of 3.59mW with resolution of 8-bit was achieved through simulations of the design. The speed was 125kHz with the supply voltage of 5V. The delay was measured in terms of clock cycle time because the layout of the architecture was not designed in this thesis. The conversion time and conversion rate was 8μs and 1MS/s respectively.

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INTRODUCTION

1.1. Introduction

The successive-approximation register analog to digital (SAR ADC) is one of the most popular approaches for implementing Analog-to-Digital converters, due to its reasonably quick conversion time, yet moderate circuit complexity. A SAR ADC applies a binary search algorithm to progressively determine the closest digital value that matches an analog input signal. A basic block diagram for an 8-bit SAR ADC consists of a comparator, Digital to Analog Converter (DAC) and successive-approximation register (SAR).

1.2. Objective

The objective of this project is to design 8-bit SAR ADC logic using TANNER S-EDIT in a HP 0.5μm SCN3M CMOS Technology. Design approach used in the project is full custom. The characteristics of SAR ADC using the designed SAR logic is to be obtained which are power consumption, resolution, speed, conversion rate and conversion time.

The 8-bit SAR logic goes to each register bit starting with the most significant bit (MSB), sets it to 1 and receives input from comparator. The input decides whether or not to keep it at 1, and goes on to the next lower bit. The processing of each bit takes one clock cycle, so that the total conversion time for an 8-bit SAR ADC will be 8 clock cycles. This conversion time will be the same regardless of the value of analog voltage. This is because the SAR logic must process each bit to see whether or not a 1 is needed.