DESIGN OF 6T MEMORY CELL AND SENSE AMPLIFIER FOR SRAM

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In the name of Allah
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ABSTRACT

This paper presents of 1bit SRAM IC design consists of SRAM cells, precharge and PMOS across amplifier using TSMC 0.25μm technology. The PMOS cross amplifier is designed to sense the signal voltage on the bit line from the memory cell for the read process because it has better output driving capability. The positive feedback of the PMOS cross coupled amplifier device accelerate the sensing speed compared to the cross coupled sense amplifier by combining the sense amplifier with complex differential logic networks. The schematics are simulated using Tanner S-Edit and T-Spice to determine the characteristics and for the comparison purpose. For layout design using Tanner L-Edit and LVS tools to get layout waveform that appropriately is same with schematic waveform.

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CHAPTER 1

INTRODUCTION

1.1 Introduction

The basic static RAM cell is shown in Figure 4. It consists of two cross-coupled inverters and two access transistors. The access transistors are connected to the word line at their respective gate terminals, and the bitlines at their source/drain terminals. The word line is used to select the cell while the bitlines are used to perform read or write operation on the cell. Internally, the cell holds the stored value on one side and its complements on the other side.

The VTC (voltage transfer characteristics) conveys the key cell design consideration for read and write operation. In the cross coupled configuration, the stored values are represented by the two stables states in the VTC. The cell will retain its current state until one of the internal nodes crosses the switching threshold. When this occurs, the cell will flip its internal state.

Due to large arrays of SRAM cells, the resulting signal, in the event of a Read operation, has a much lower voltage swing. To compensate for that swing a sense amplifier is used to amplify voltage coming off Bit Line and Bit Line. The voltage coming out of the sense amplifier typically has a fully swing (0 – 5.0V) voltage. Sense amplifier also helps reduce the delay times and power consumption in the overall SRAM chip.

Read/Write

During a read operation these two bit lines are connected to the sense amplifier that recognizes if a logic data "1" or "0" is stored in the selected elementary cell. This sense amplifier then transfers the logic state to the output buffer which is