CHARACTERIZATION OF 50nm NMOSFET

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ABSTRACT

This paper presents a detailed study of characteristic of 50nm MOSFET by using SILVACO TCAD tool. The gate length (*L*) is reducing into 50nm based on conventional 0.3μm NMOSFET. The result of performance between two structures is compared by using Atlas simulation. The analysis is focused on I_d-V_g and I_d-V_d characteristic on the two gate length as mentioned. ATHENA and ATLAS in SILVACO TCAD tool was used to construct and analyze the semiconductor device. The result has shown how the drain current increase steadily and improvement on threshold voltage by 50nm NMOS in comparison with 0.3μm technology.

Keyword- 50nm NMOS, I_d-V_g, I_d-V_d, Simulation

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CHAPTER 1

INTRODUCTION

1.1 History Background of MOSFET

MOS transistor based integrated circuits have transformed the world we live in. It is estimated that there are more than 15 billion silicon semiconductor chips currently in use with an additional 500,000 sold each day [1]. The ever shrinking size of the MOS transistors that result in faster, smaller, and cheaper systems have enabled ubiquitous use of these chips. Among these semiconductor chips, a prevalent component is the high-performance general-purpose microprocessor. Figure 1-1 illustrates the timeline on technology scaling and new high performance microprocessor architecture introductions in the past three decades [3].

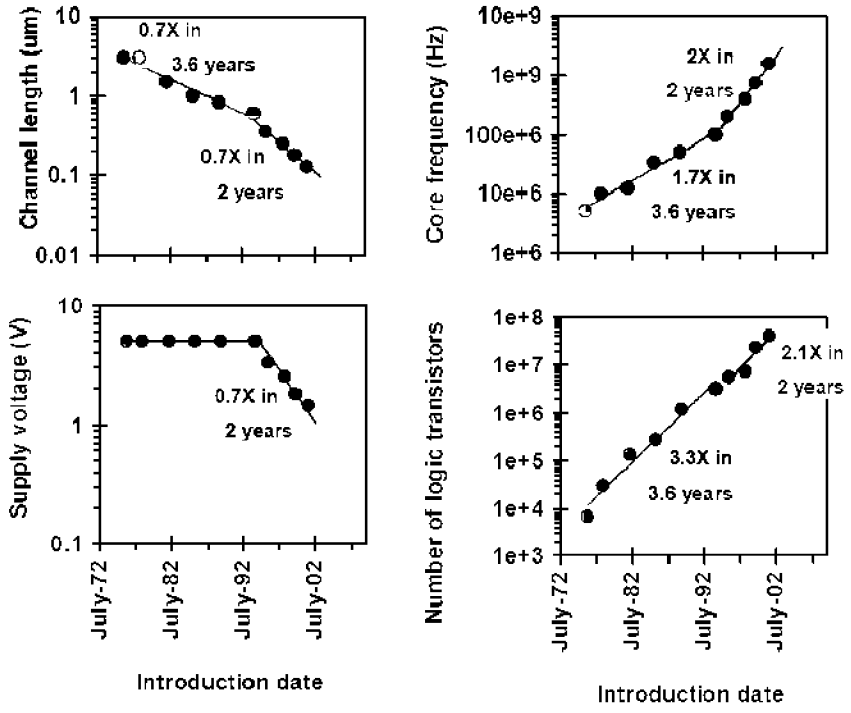

Figure 1-1: Timeline on technology scaling and new microprocessor architecture introduction.