ANALYSIS AND DESIGN OF A LOW POWER, HIGH SPEED SAMPLE AND HOLD CIRCUIT FOR PIPELINED ADC USING 0.18μm CMOS TECHNOLOGY

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UNIVERSITI TEKNOLOGI MARA

SUHAIB BIN MOHD TARMIZI
FACULTY OF ELECTRICAL ENGINEERING
UNIVERSITI TEKNOLOGI MARA
40450 SHAH ALAM SELANGOR
MALAYSIA
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ABSTRACT

This paper present an analysis and design of Sample and Hold (SH) circuit for front end block pipelined ADC using 0.18µm CMOS technology. The objective of this project is to design a sample and hold circuit and analyzing in term of low power and high speed with two different topologies, which are two stage operational amplifier and folded cascode operational amplifier. The analysis of op amp parameters is done for 0.18µm CMOS technology. SILVACO EDA tools have been used for schematic design and simulation. Complete Sample and Hold circuit has been designed with 1.8V Vpp, 1.8V voltage supply and 5Mz sampling frequency. The power consumption for two stage operational amplifiers is 0.081mW and for folded cascode operational amplifier is 0.593mW. The propagation delay of the circuit is 131.15ns for two stage operational amplifier and 2.7402ns for folded cascode operational amplifier. Based on the analysis and design, two stage operational amplifier can give low power consumption and low speed while folded cascode operational amplifier can give high power consumption but high speed.

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CHAPTER 1

INTRODUCTION

1.1 INTRODUCTION

With the demand for pipelined Analog Digital Converter (ADC) has increased rapidly with the growth of technology [1], with having various advantages including as an alternative solution for wireless communication system, the performance of Sample and Hold (SH) circuit in pipeline ADC will take into consideration as the SH circuit play the main part in the ADC which the performance of the SH circuit will affect the whole ADC [2]. In other hand, power consumption and speed of the SH circuit will be the main focus during the circuit design as these two factors has become the major problem and typically the pipelined analog to digital converter are used for the applications that requires low power and high speed.

The software used in this project is SILVACO EDA Tool by using 0.18μm CMOS technology. SILVACO delivers a comprehensive set of leading edge TCAD and EDA tools. The SILVACO Gateway is used to design a schematic and support flat or hierarchical designs of any technology. The advantages of using Gateway is, it can be used by large design teams through global preferences and handles multiple designs and technologies with specific workspaces.